ECONOLITE ASC/3-2070
OVERLAP PROGRAMMING DETAIL
(program controller as shown)

1. From Main Menu select 2. CONTROLLER

2. From CONTROLLER Submenu select 2. VEHICLE OVERLAPS

3. Press "Toggle" until positioned on Overlap F

OVERLAP F
Select TMG VEH OVLP [F] and 'NORMAL'

```
TMG VEH OVLP...[F] TYPE: ...... NORMAL
   PHASES 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
INCLUDED . . X . . . . . . . . . . . . .

LAG GRN 0.0 YEL 0.0 RED 0.0
```
Toggle Once

OVERLAP G
Select TMG VEH OVLP [G] and 'NORMAL'

```
TMG VEH OVLP...[G] TYPE: ...... NORMAL
   PHASES 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
INCLUDED X . . . . . . . . . . . . . . .

LAG GRN 0.0 YEL 0.0 RED 0.0
```
Toggle Once

OVERLAP H
Select TMG VEH OVLP [H] and 'NORMAL'

```
TMG VEH OVLP...[H] TYPE: ...... NORMAL
   PHASES 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
INCLUDED . . X . . . . . . . . . . . . .

LAG GRN 0.0 YEL 0.0 RED 0.0
```
Press Toggle until
positioned over Overlap A

OVERLAP A
Select TMG VEH OVLP [A] and 'PPLT FYA'

```
TMG VEH OVLP...[A] TYPE: .... PPLT FYA

PROTECTED RIGHT TURN.... PHASE    1
OPPOSING THROUGH.......  PHASE    2

FLASHING ARROW OUTPUT.....CH9 ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE........... 0
```
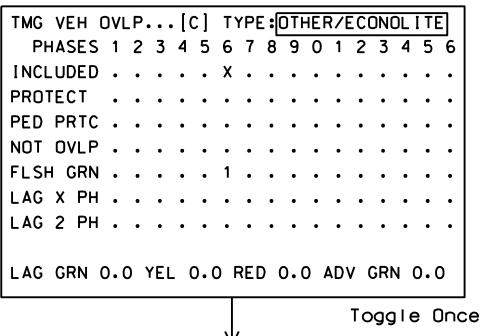Toggle Once

OVERLAP B
Select TMG VEH OVLP [B] and 'PPLT FYA'

```
TMG VEH OVLP...[B] TYPE: .... PPLT FYA

PROTECTED RIGHT TURN.... OVERLAP  G
OPPOSING THROUGH.......  PHASE    3

FLASHING ARROW OUTPUT.....CH10 ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE........... 0
```
Toggle Once

OVERLAP C
Select TMG VEH OVLP [C] and 'OTHER/ECONOLITE'

```
TMG VEH OVLP...[C] TYPE: OTHER/ECONOLITE
   PHASES 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
INCLUDED . . . . . X . . . . . . . . . .
PROTECT  . . . . . . . . . . . . . . . .
PED PRTC . . . . . . . . . . . . . . . .
NOT OVLP . . . . . . . . . . . . . . . .
FLSH GRN . . . . . 1 . . . . . . . . . .
LAG X PH . . . . . . . . . . . . . . . .
LAG 2 PH . . . . . . . . . . . . . . . .

LAG GRN 0.0 YEL 0.0 RED 0.0 ADV GRN 0.0
```
Toggle Once

OVERLAP D
Select TMG VEH OVLP [D] and 'PPLT FYA'

```
TMG VEH OVLP...[D] TYPE: .... PPLT FYA

PROTECTED RIGHT TURN....  OVERLAP  H
OPPOSING THROUGH.......   PHASE    2

FLASHING ARROW OUTPUT.....CH12 ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE........... 0
```
END PROGRAMMING

ASC/3 FLASH SENSE INPUT CONTROL
FOR RED-RED FLASH

*The NCDOT default database is programmed to addresss Yellow-Red flash.
Logic Statement 100 must be modified as shown when running Red-Red flash.

1. From Main Menu select 1. CONFIGURATION

2. From CONFIGURATION Submenu select 8. LOGIC PROCESSOR

3. From LOGIC PROCESSOR Submenu select 2. LOGIC STATEMENTS

Change the "LP" to 100 and move the cursor down. Delete
the two "CTR-SET" statements by moving the cursor over
them and hitting the "C" key, then hit "ENTER", select
"LP SET CIB ON", hit "ENT", and then set the number to 427.

```
LP#:100  COPY FROM:100  ACTIVE: M   FALSE
IF   LP CIB CODE ON                331  F

THEN LP  DELAY FOR         1.0 SECONDS
     LP  SET CIB ON        427

ELSE
```
THIS STATEMENT IS USED
TO CONTROL THE FLASH
SENSE INPUT WHEN RUNNING
RED-RED FLASH OPERATION.

Hit "ESC", then 1 for "LOGIC STATEMENT CONTROL",
next verify that LP#100 is ENABLED.

END PROGRAMMING

FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE
SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

1. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.

2. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.

3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS
TO FLASHER UNIT 1.
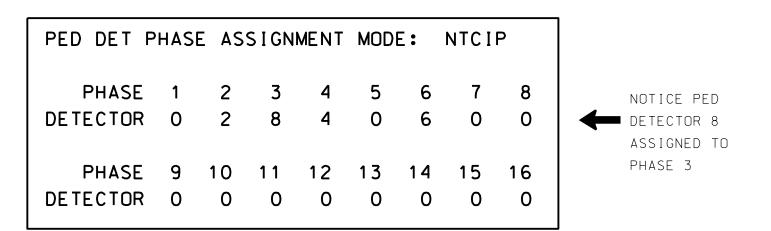
ECONOLITE ASC/3-2070
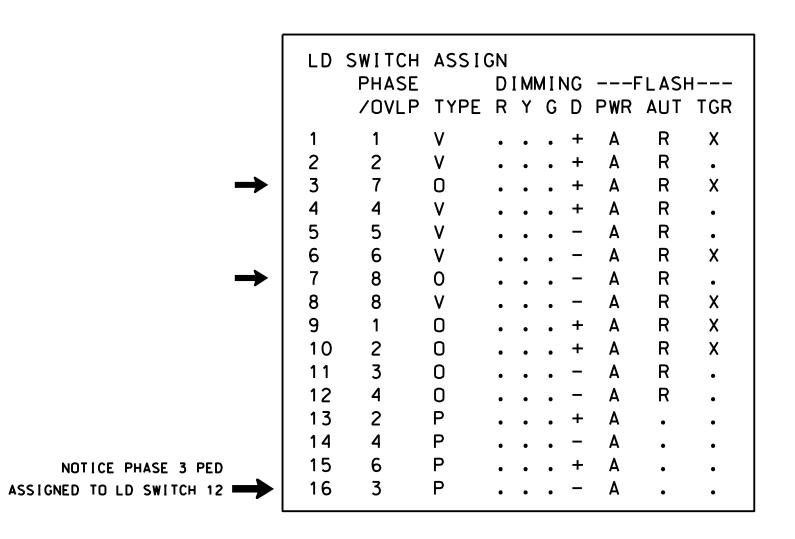## LOAD SWITCH AND
PED 3 PROGRAMMING ASSIGNMENT DETAIL
(program controller as shown)

1. From Main Menu select 6. DETECTORS

2. From DETECTOR Submenu select 3. PED DETECTOR INPUT ASSIGNMENT

```
PED DET PHASE ASSIGNMENT MODE:  NTCIP

      PHASE    1   2   3   4   5   6   7   8
   DETECTOR    0   2   8   4   0   6   0   0

      PHASE    9  10  11  12  13  14  15  16
   DETECTOR    0   0   0   0   0   0   0   0
```
NOTICE PED
DETECTOR 8
ASSIGNED TO
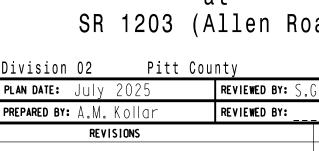PHASE 3

To assign load switch S4 as OLG, program LD SWITCH 3
as OVLP '7' TYPE 'O' as shown below.
To assign load switch S10 as OLH, program LD SWITCH 7
as OVLP '8' TYPE 'O' as shown below.
To reassign load switch S12 as PED 3, program LD SWITCH 16
as '3' TYPE 'P' as shown below.

1. From Main Menu select 1. CONFIGURATION

2. From CONFIGURATION Submenu select 3. LOAD SW ASSIGN

LD SWITCH ASSIGN

PHASE /OVLP	TYPE	DIMMING R	Y	G	D	FLASH PWR	AUT	TGR
1	1	V	.	.	.	+	A	R	X
2	2	V	.	.	.	+	A	R	X
3	7	O	.	.	.	+	A	R	X
4	4	V	.	.	.	+	A	R	.
5	5	V	.	.	.	-	A	R	.
6	6	V	.	.	.	-	A	R	X
7	8	O	.	.	.	-	A	R	.
8	8	V	.	.	.	-	A	R	X
9	1	O	.	.	.	+	A	R	X
10	2	O	.	.	.	+	A	R	X
11	3	O	.	.	.	-	A	R	.
12	4	O	.	.	.	-	A	R	.
13	2	P	.	.	.	+	A	.	.
14	4	P	.	.	.	-	A	.	.
15	6	P	.	.	.	+	A	.	.
16	3	P	.	.	.	-	A	.	.

NOTICE PHASE 3 PED
ASSIGNED TO LD SWITCH 12

THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 02-0500T2
DESIGNED: July 2025
SEALED: 07/15/2025
REVISED: N/A

Temporary Signal 2 - TMP Phase III
Electrical Detail - Sheet 2 of 2

DOCUMENT NOT CONSIDERED FINAL
UNLESS ALL SIGNATURES COMPLETED

SR 1467 (Stantonsburg Road)
at
SR 1203 (Allen Road)

Division 02	Pitt County	Greenville
PLAN DATE: July 2025	REVIEWED BY: S.G. Haynie	
PREPARED BY: A.M. Kollar	REVIEWED BY:	

SEAL

NORTH CAROLINA
PROFESSIONAL
ENGINEER
SEAL
029531
Steven G. Haynie

REVISIONS	INIT.	DATE

SIGNATURE   DATE
SIG. INVENTORY NO.   02-0500T2

Steven G. Haynie 7/15/2025