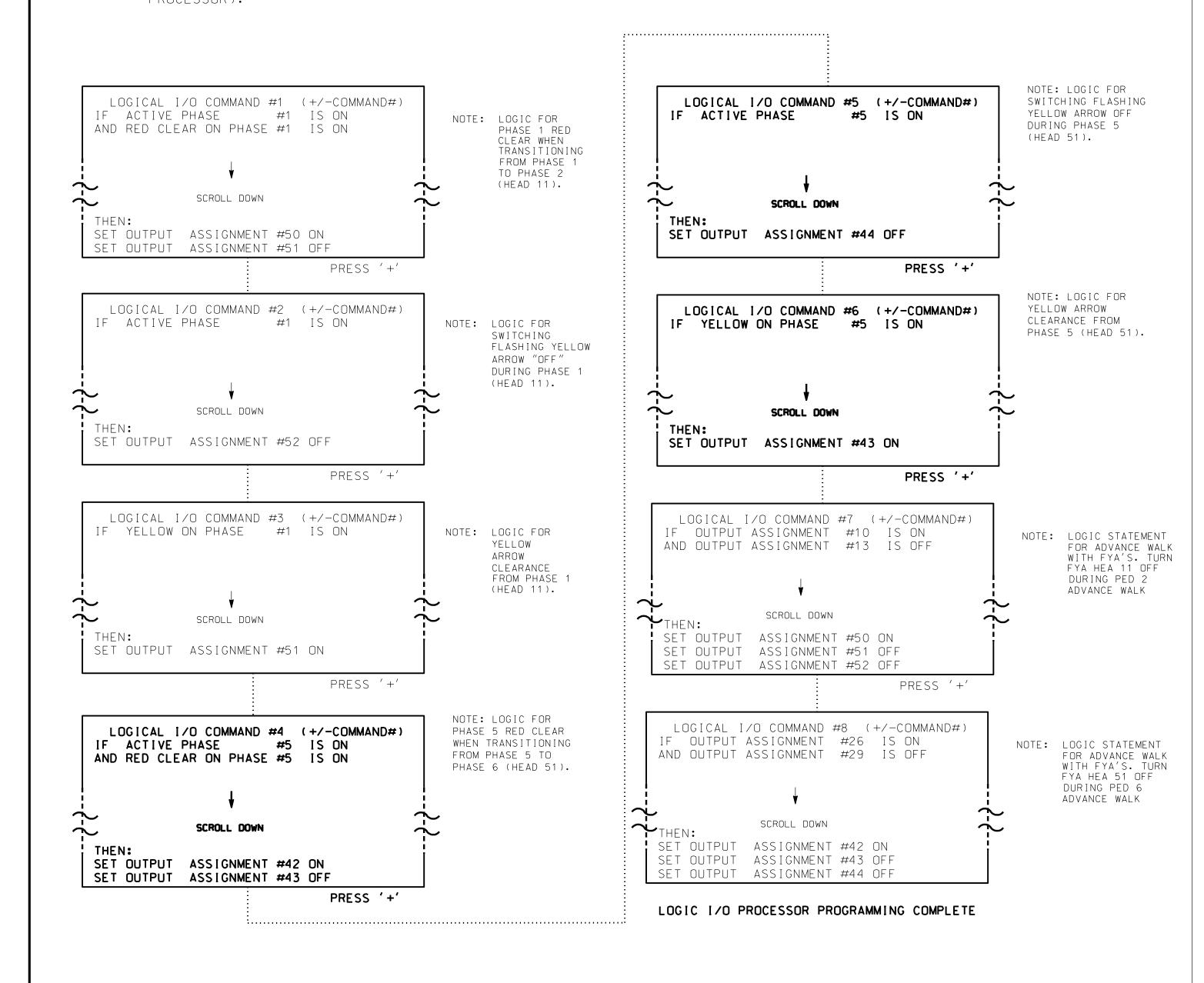
## U-5789

## LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS), SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, AND 8.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



OUTPUT REFERENCE SCHEDULE USE TO INTERPRET LOGIC PROCESSOR OUTPUT 10 = Phase 2 WALK OUTPUT 13 = Phase 2 Green OUTPUT 26 = Phase 6 WALK OUTPUT 29 = Phase 6 Green OUTPUT 42 = Overlap C Red OUTPUT 43 = Overlap C Yellow OUTPUT 44 = Overlap C Green OUTPUT 50 = Overlap A Red OUTPUT 51 = Overlop A Yellow OUTPUT 52 = Overlap A Green

## ALTERNATE PHASING ACTIVATION DETAIL

TO RUN ALT. PHASING DURING <u>COORDINATION</u> - SELECT ALL PAGE CHANGES (AS SHOWN BELOW) WITHIN COORDINATION PLAN PROGRAMMING.

TO RUN ALT. PHASING DURING FREE RUN - PROGRAM PAGE CHANGES (SHOWN BELOW) IN SEPARATE TIME OF DAY EVENTS. IF PAGE 1 IS USED, NO EVENT PROGRAMMING IS NECESSARY FOR THAT PARTICULAR PAGE.

PHAS I NG	INPUTS PAGE	OVERLAPS PAGE
ACTIVE PAGES REQUIRED TO RUN <u>DEFAULT PHASIN</u> G	1	1
ACTIVE PAGES REQUIRED TO RUN ALTERNATE PHASING	2	2

NOTE: PAGES NOT SHOWN (i.e. sequence, phase control, etc.) SHOULD REMAIN AS '1', OR AS DEFINED BY TIMING ENGINEER.

IMPORTANT: IF ALT. PHASING IS USED DURING FREE RUN AND COORDINATION, DO NOT OPERATE TIME OF DAY PAGE CHANGE EVENTS CONCURRENTLY WITH COORDINATION PLAN EVENTS IN THE EVENT SCHEDULER. (EX. FREE RUN PAGE CHANGE EVENT SHOULD END BEFORE COORDINATION PLAN EVENT STARTS AND VICE-VERSA).

## ALTERNATE PHASING PAGE CHANGE SUMMARY

THE FOLLOWING IS A SUMMARY OF WHAT TAKES PLACE WHEN THESE OVERLAP/INPUT PAGE CHANGES ACTIVATE TO CALL THE "ALTERNATE PHASING":

OVERLAPS PAGE 2: Modifies overlap parent phases

for heads 11 and 51 to run protected

turns only.

INPUTS PAGE 2:

Disables phase 6 call on loop 1A and reduces delay time for phase 1

call on loop 1A to 0 seconds.

Disables phase 2 call on loop 5A and reduces delay time for phase 5 call on loop 5A to 0 seconds.

**DAVENORT** 

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THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: Ø3-Ø896 DESIGNED: May 2025 SEALED: 7/2/2025 REVISED: N/A

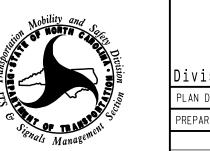
Project #: 230907 Electrical Details

Final Design - Sheet 6 of 7

ELECTRICAL AND PROGRAMMING

750 N.Greenfield Pkwy, Garner, NC 27529

NC 53 (Western Boulevard)



Gateway South Division 3 Onslow County Jacksonville May 2025 D. Bennett PLAN DATE: REVIEWED BY: PREPARED BY: B. Dowell REVIEWED BY: REVISIONS INIT. DATE

020608 Donald Kill Burnelt !!

SIG. INVENTORY NO. 03-0896

DOCUMENT NOT CONSIDERED

FINAL UNLESS ALL

SIGNATURES COMPLETED

SEAL