

(program controller as shown)

- Toggle to 'Overlap F'
- OVERLAP F

```

TMG VEH OVLP...[F] TYPE: .....NORMAL
  PHASES 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
INCLUDED . . . . X . . . . . . . . . .
LAG GRN 0.0 YEL 0.0 RED 0.0

```

Toggle Once

OVERLAP G

```

TMG VEH DVL P...[G] TYPE: .....NORMAL
  PHASES 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
INCLUDED . . X . . . . . . . . . .
LAG GRN 0.0 YEL 0.0 RED 0.0

```

Toggle Once

OVERLAP H.

```

TMG VEH DVL P...[H] TYPE: .....NORMAL
  PHASES 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
INCLUDED . . . . X . . . . . . . . .
LAG GRN 0.0 YEL 0.0 RED 0.0

```

Toggle to 'Overlap B'

OVERLAP E

TMG	VEH	DVLP...	[B]	TYPE:	OTHER/ECONDLITE											
PHASES	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6
INCLUDED	X	.	X
PROTECT
PED PRTC
NOT DVLP
FLSH GRN	1	.	1
LAG X PH
LAG 2 PH
LAG GRN	0.0	YEL	0.0	RED	0.0	ADV	GRN	0.0								

Toggle Once

OVERLAP C

```

TMG VEH OVLP...[C] TYPE: ....[PPLT FYA]
PROTECTED LEFT TURN....    OVERLAP    G
OPPOSING THROUGH.....    PHASE      2

FLASHING ARROW OUTPUT.....CH11 ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE..... 0

```

Toggle Once

OVERLAP [

```

TMG VEH OVLP...[D] TYPE: ....[PPLT FYA]
PROTECTED LEFT TURN....    OVERLAP    H
OPPOSING THROUGH.....    PHASE      4

FLASHING ARROW OUTPUT.....CH12 ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE.....0

```

END PROGRAMMING

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

1. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
2. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

Countdown Ped Signals are required to display timing only during Ped Clearance Interval. Consult Ped Signal Module user's manual for instructions on selecting this feature.

THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 07-1118
DESIGNED: January 2025
SEALED: 03-14-2025
REVISED: N/A