The following logic processor configuration holds the FYA on signal head 11 red for the duration of the delayed green time (leading ped interval) when serving a ped call on the opposing through phase and serve phase 4 instead of phase 3 if there is a phase 4 ped call.

1. From Main Menu select | 1. CONFIGURATION

2. From CONFIGURATION Submenu select | 8. LOGIC PROCESSOR

3. From the LOGIC PROCESSOR Submenu select 2. LOGIC STATEMENTS

ENTER A "1" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#:	1	COPY FROM:	1	ACTIVE:	М	(T/F)
I F AND		ON PH WALK GREEN ON PH		2 2	IS IS	ON OF F
THEN	SIG	SET OLP RED SET OLP YELL SET OVLP GRE		1 1 1		ON OFF OFF
ELSE						

HOLD SIGNAL HEAD 11 FYA RED DURING THE PHASE 2 DELAYED GREEN TIME (LEADING PED INTERVAL)

ENTER A "2" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#:	2	COPY FROM:	2	ACTIVE:	М	(T/F)	
ΙF	CTR	ON PH PED CHK		4	IS	ON	
THEN	CTR	OMIT PHASE		3		ON	
ELSE							

LOGIC TO SERVE PHASE 4 INSTEAD OF PHASE 3 IF THERE IS A PHASE 4 PED CALL.

1. From Main Menu select | 1. CONFIGURATION

2. From CONFIGURATION Submenu select 8. LOGIC PROCESSOR

3. From the LOGIC PROCESSOR Submenu select | 1. LOGIC STATEMENT CONTROL

ENABLE LOGIC PROCESSOR STATEMENTS 1-4 BY POSITIONING THE CURSOR OVER THE FIELDS SHOWN BELOW AND USING THE TOGGLE KEY TO ENABLE THEM .

LOGIC STA	CO	CONTROL														
	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6
LP 1-15	Ε	Ε	•	•	•	•	•	•	•	•	•	•	•	•	•	•
LP 16-30	•	•	•	•		•	•	•	•	•	•	•			•	•
LP 31-45	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
LP 46-60		•	•	•	•	•	•	•	•	•	•	•	•		•	•
LP 61-75	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
LP 76-90	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

END PROGRAMMING

ECONOLITE ASC/3-2070 BACKUP PROTECTION ENABLE PROGRAMMING

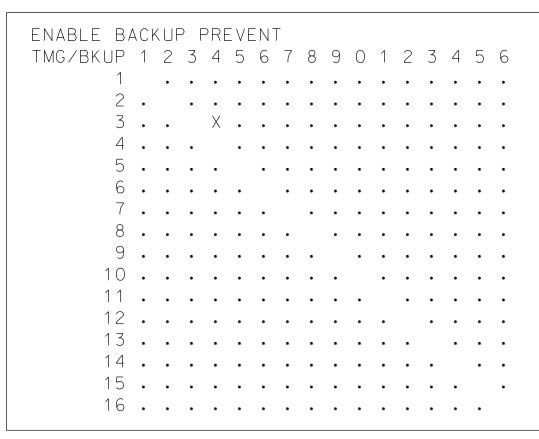
(program controller as shown)

1. From Main Menu select | 1. CONFIGURATION

2. From CONFIGURATION Submenu select | 1. CONTROLLER SEQ

3. From CONTROLLER SEQUENCE Submenu select | 3. BACKUP PREVENT PHASES |

Follow programming as shown below. On the 'ENABLE BACKUP PREVENT' screen move cursor to the appropriate field and press 'YES/NO' on the controller keypad to toggle field value between 'X' and 'OFF'.



END PROGRAMMING

NOTES

'TIMING' (row) phase is active or next.

ASC/3 FLASH SENSE INPUT CONTROL FOR RED-RED FLASH

*The NCDOT default database is programmed to addresss Yellow-Red flash. Logic Statement 100 must be modified as shown when running Red-Red flash.

1. From Main Menu select | 1. CONFIGURATION

2. From CONFIGURATION Submenu select 8. LOGIC PROCESSOR

3. From LOGIC PROCESSOR Submenu select 2. LOGIC STATEMENTS

Change the "LP" to 100 and move the cursor down. Delete the two "CTR-SET" statements by moving the cursor over them and hitting the "C" key. then hit "ENTER", select "LP SET CIB ON", hit "ENT", and then set the number to 427.

LP#:100 COPY FROM:100 ACTIVE: M FALSE IF LP CIB CODE ON 331 F SENSE INPUT WHEN RUNNING RED-RED FLASH OPERATION. THEN LP DELAY FOR 1.0 SECONDS 427 LP SET CIB ON ELSE

Hit "ESC", then 1 for "LOGIC STATEMENT CONTROL", next verify that LP#100 is ENABLED.

END PROGRAMMING

⁻AtkinsRéalis 1616 EAST MILLBROOK ROAD. SUITE 160 RALEIGH, NORTH CAROLINA 27609 (919) 876-6888 NCBEES #F-0326

THIS STATEMENT IS USED

TO CONTROL THE FLASH

PROJECT REFERENCE NO. U-4758 | Sig. 15.4

ECONOLITE ASC/3-2070 STARTUP AND SOFTWARE FLASH PROGRAMMING DETAIL

(program controller as shown)

1. From Main Menu select 2. CONTROLLER

2. From CONTROLLER Submenu select | 5. START/FLASH

START/FLASH DATA ----START UP-----1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 PHASE A B C D E F G H I J K L M N O P FLASH>MON. NO FL TIME.. O ALL RED... 6 PWR START SEQ.. 1 MUTCD→ YES Y-G: NO

Scroll down on this screen and set "Exit FI" to Green "G"

COUNTDOWN PEDESTRIAN SIGNAL OPERATION

Countdown Ped Signals are required to display timing only during Ped Clearance Interval. Consult Ped Signal Module user's manual for instructions on selecting this feature.

FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

1. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.

2. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.

3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: Ø7-1114 DESIGNED: January 2025 SEALED: 03-14-2025 REVISED: N/A

Electrical Detail - Sheet 4 of 4

ELECTRICAL AND PROGRAMMING Prepared for the Offices of:

SR 1820 (Sandy Ridge Road)

SR 1837 (Clinard Farms Road)

Division 7 Guilford County PLAN DATE: January 2025 REVIEWED BY: AM Encarnacion PREPARED BY: JT Stiff REVIEWED BY: PL Alexander

SIG. INVENTORY NO. 07-1114

DOCUMENT NOT CONSIDERED

FINAL UNLESS ALL

SIGNATURES COMPLETED

REVISIONS INIT. DATE

1. 'X' inhibits the controller from servicing the 'BACKUP' (column) phase when the