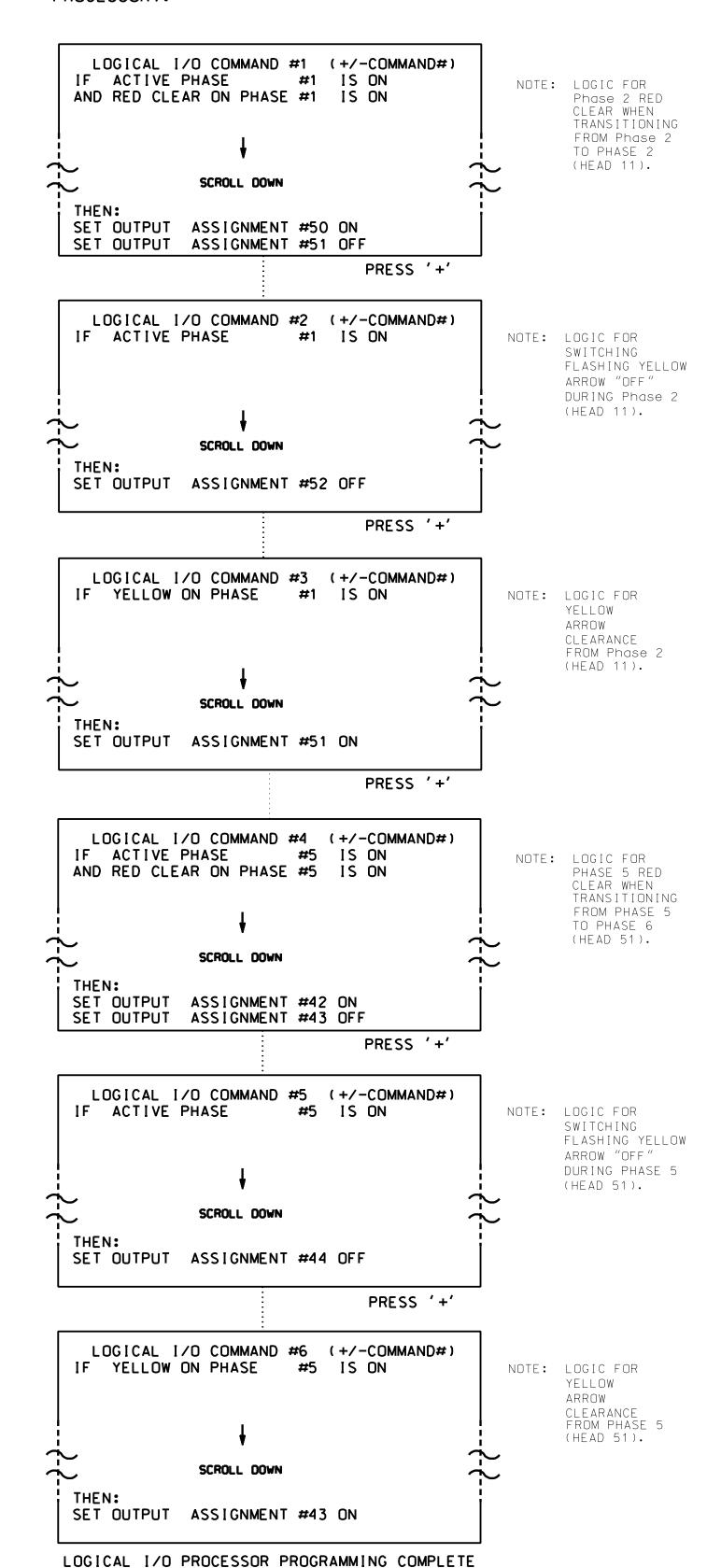
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL

TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, AND 6.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



OVERLAP PROGRAMMING DETAIL FOR DEFAULT PHASING

(program controller as shown below)

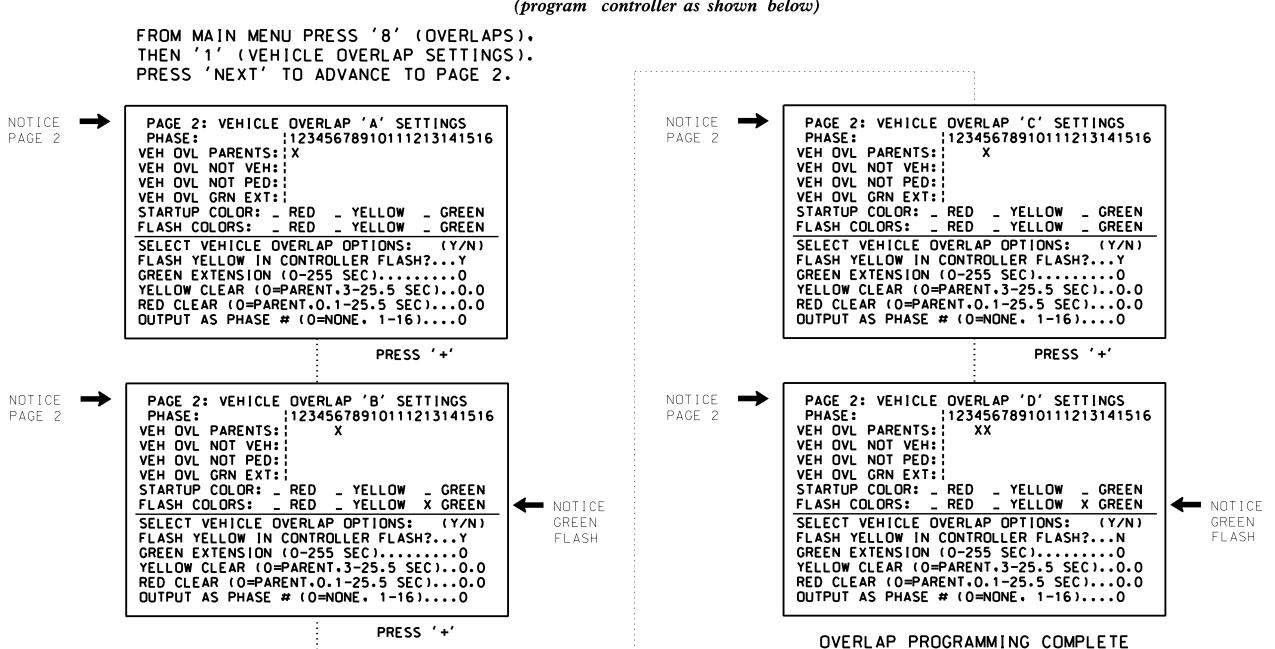
FROM MAIN MENU PRESS '8' (OVERLAPS).

PRESS '+'

THEN '1' (VEHICLE OVERLAP SETTINGS). PAGE 1: VEHICLE OVERLAP 'C' SETTINGS PAGE 1: VEHICLE OVERLAP 'A' SETTINGS 112345678910111213141516 112345678910111213141516 VEH OVL PARENTS: XX VEH OVL PARENTS: VEH OVL NOT VEH: !
VEH OVL NOT PED: ! VEH OVL NOT VEH: VEH OVL NOT PED: VEH OVL GRN EXT: VEH OVL GRN EXT: : STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW X GREEN STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW X GREEN SELECT VEHICLE OVERLAP OPTIONS: (Y/N) GREEN SELECT VEHICLE OVERLAP OPTIONS: (Y/N) GREEN FLASH YELLOW IN CONTROLLER FLASH?...Y FLASH FLASH YELLOW IN CONTROLLER FLASH?...Y FLASH GREEN EXTENSION (0-255 SEC)..... GREEN EXTENSION (0-255 SEC)..... YELLOW CLEAR (0=PARENT.3-25.5 SEC)..0.0 YELLOW CLEAR (0=PARENT.3-25.5 SEC)..0.0 RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0 RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0 OUTPUT AS PHASE # (0=NONE. 1-16)....0 PRESS '+' PRESS '+' PAGE 1: VEHICLE OVERLAP 'D' SETTINGS PAGE 1: VEHICLE OVERLAP 'B' SETTINGS 12345678910111213141516 12345678910111213141516 VEH OVL PARENTS: | XX VEH OVL PARENTS: VEH OVL NOT VEH: VEH OVL NOT VEH: VEH OVL NOT PED: | VEH OVL GRN EXT: | VEH OVL NOT PED: :
VEH OVL GRN EXT: : STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW X GREEN STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW X GREEN SELECT VEHICLE OVERLAP OPTIONS: (Y/N) SELECT VEHICLE OVERLAP OPTIONS: (Y/N) GREEN GREEN FLASH YELLOW IN CONTROLLER FLASH?...Y FLASH YELLOW IN CONTROLLER FLASH?...N FLASH FLASH GREEN EXTENSION (0-255 SEC).....0 GREEN EXTENSION (0-255 SEC)..... YELLOW CLEAR (0=PARENT.3-25.5 SEC)..0.0 YELLOW CLEAR (0=PARENT.3-25.5 SEC)..0.0 RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0 RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)...0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

OVERLAP PROGRAMMING DETAIL FOR ALTERNATE PHASING

(program controller as shown below)



Signal Upgrade - Final Design Electrical Detail - Sheet 2 of 5

OVERLAP PROGRAMMING COMPLETE

DESIGNED: May 2022 SEALED: 5/17/2024 REVISED:

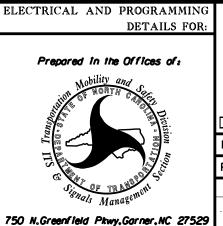
THIS ELECTRICAL DETAIL IS FOR

THE SIGNAL DESIGN: 03-0893

PROJECT REFERENCE NO.

U-6202

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



SR 2048 (Gordon Rd) SR 1328 (White Rd)

ivision 3 New Hanover County Wilmingtor August 2023 REVIEWED BY: N.K. Vlanich PLAN DATE: PREPARED BY: E.E. Tiller REVIEWED BY: N.R. Simmons REVISIONS INIT. DATE

TH CARO OR OFESSION 1 031464 COUNTER Notasha R Simmons 5/17/202 SIGNATURE DATE SIG. INVENTORY NO. 03-0893

HNTB NORTH CAROLINA, P.C.

OUTPUT REFERENCE SCHEDULE

USE TO INTERPRET LOGIC PROCESSOR

OUTPUT 43 = Overlap C Yellow

OUTPUT 51 = Overlap A Yellow OUTPUT 52 = Overlap A Green

OUTPUT 44 = Overlap C Green

OUTPUT 42 = Overlap C Red

OUTPUT 50 = Overlap A Red

HNTB NURTH CARULINA, F.C. 343 E. Six Forks Road, Suite 200 Raleigh, North Carolina 27609 NC License No: C-1554 (919) 546-8997