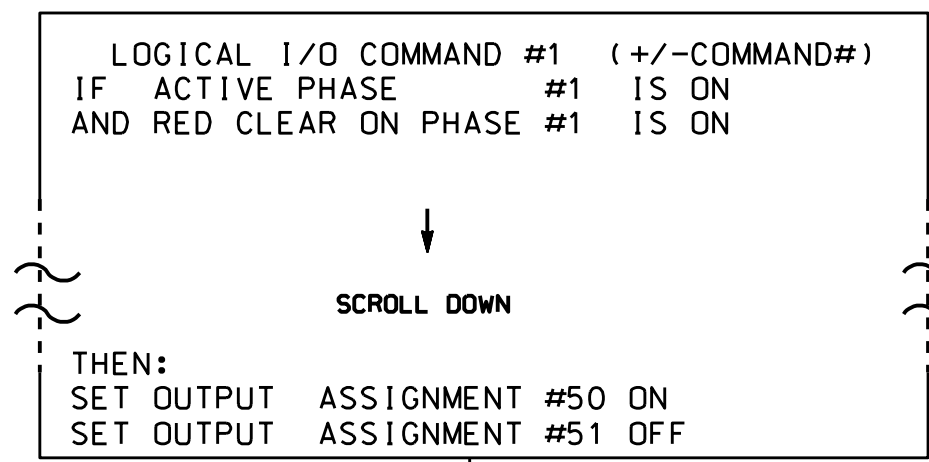


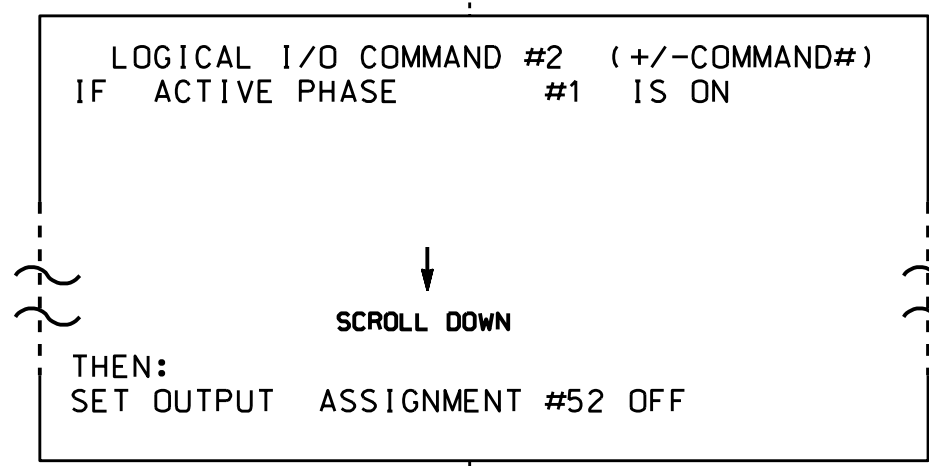
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

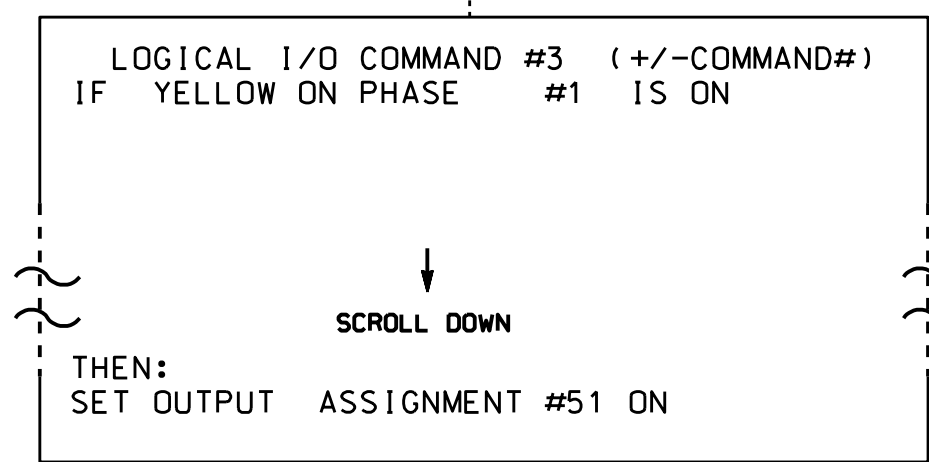
1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2 AND 3.
2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



NOTE: LOGIC FOR PHASE 1 RED CLEAR WHEN TRANSITIONING FROM PHASE 1 TO PHASE 2 (HEAD 11).



NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW OFF DURING PHASE 1 (HEAD 11).



NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 1 (HEAD 11).

LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OUTPUT REFERENCE SCHEDULE	
USE TO INTERPRET LOGIC PROCESSOR	
OUTPUT 50 =	Overlap A Red
OUTPUT 51 =	Overlap A Yellow
OUTPUT 52 =	Overlap A Green

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

```

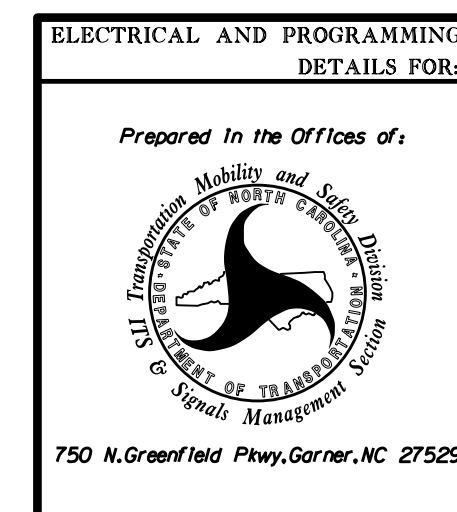
PAGE 1: VEHICLE OVERLAP 'A' SETTINGS
PHASE:           ;12345678910111213141516
VEH OVL PARENTS:;XX
VEH OVL NOT VEH:;
VEH OVL NOT PED:;
VEH OVL GRN EXT:;
STARTUP COLOR:  _ RED  _ YELLOW  _ GREEN
FLASH COLORS:   _ RED  _ YELLOW  X GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0-255 SEC)...0
YELLOW CLEAR (0=PARENT.3-25.5 SEC)...0.0
RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE. 1-16)...0
  
```

← NOTICE GREEN FLASH

OVERLAP PROGRAMMING COMPLETE

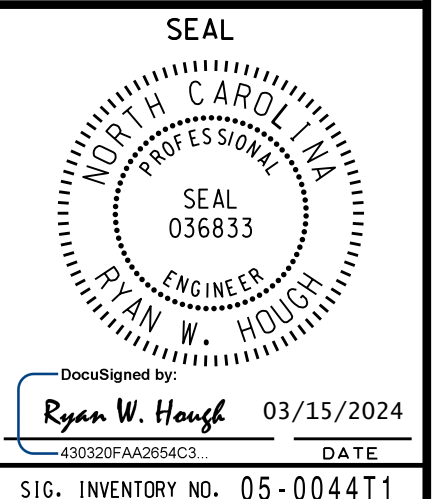
THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 05-0044T1
DESIGNED: February 2024
SEALED: 03/14/2024
REVISED: N/A

Electrical Detail - Sheet 2 of 2



NC 56 at I-85 SB Ramps	
Division 5 Granville County Butler	
PLAN DATE: March 2024	REVIEWED BY:
PREPARED BY: S.Kirkpatrick	REVIEWED BY:
REVISIONS	INIT. DATE

DOCUMENT NOT CONSIDERED
FINAL UNLESS ALL
SIGNATURES COMPLETED



DocuSigned by:
Ryan W. Hough 03/15/2024
430320FAA2854C3 DATE
SIG. INVENTORY NO. 05-0044T1