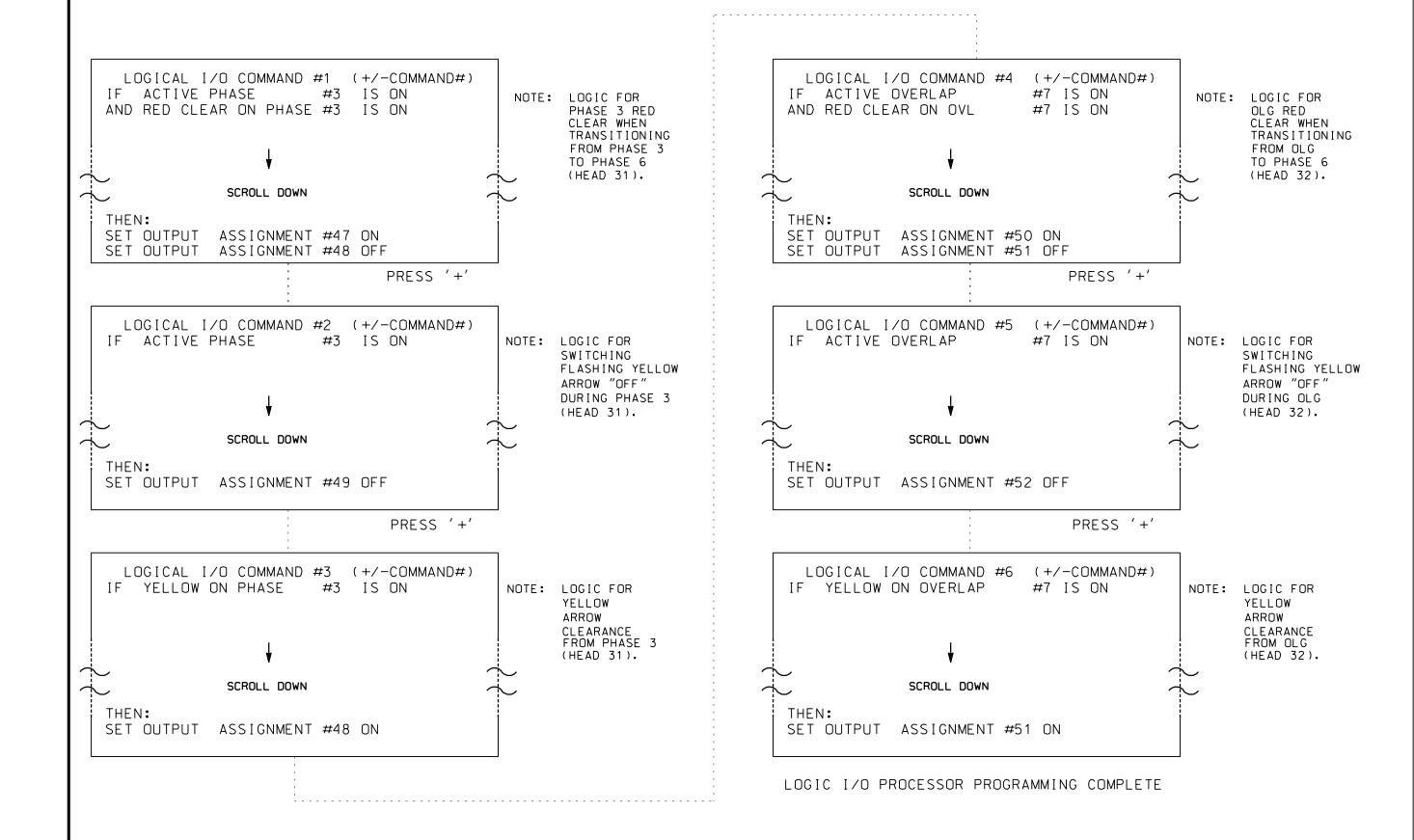
# LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

#### (program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1,2,3,4,5 AND 6.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).

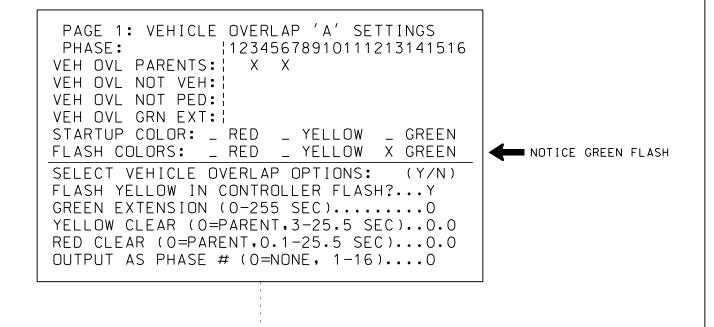


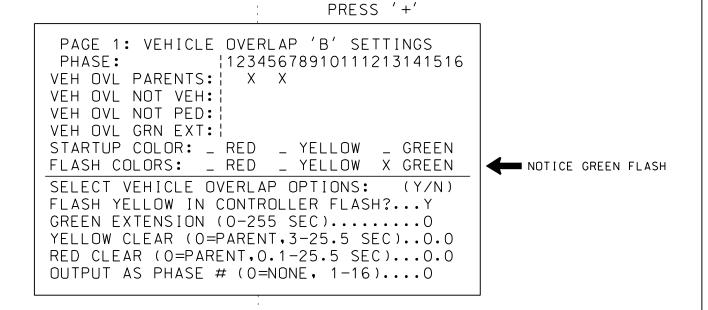
### **OUTPUT REFERENCE SCHEDULE** OUTPUT 47 = Overlap B Red OUTPUT 48 = Overlap B Yellow OUTPUT 49 = Overlap B Green OUTPUT 50 = Overlap A Red OUTPUT 51 = Overlap A Yellow OUTPUT 52 = Overlap A Green

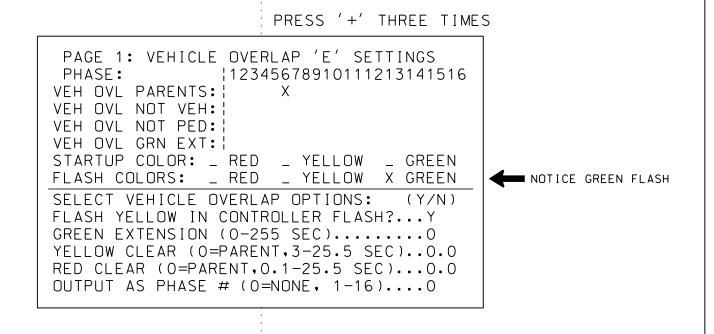
## OVERLAP PROGRAMMING DETAIL FOR DEFAULT PHASING

#### (program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).







PRESS '+' TWO TIMES
PAGE 1: VEHICLE OVERLAP 'G' SETTINGS PHASE:  12345678910111213141516 VEH OVL PARENTS:   X VEH OVL NOT VEH:   VEH OVL NOT PED:   VEH OVL GRN EXT:   STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW _ GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?N GREEN EXTENSION (0-255 SEC)0 YELLOW CLEAR (0=PARENT,3-25.5 SEC)0.0 RED CLEAR (0=PARENT,0.1-25.5 SEC)0.0 OUTPUT AS PHASE # (0=NONE, 1-16)0

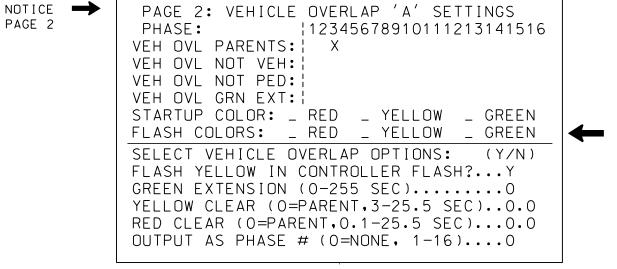
OVERLAP G PROGRAMMING COMPLETE

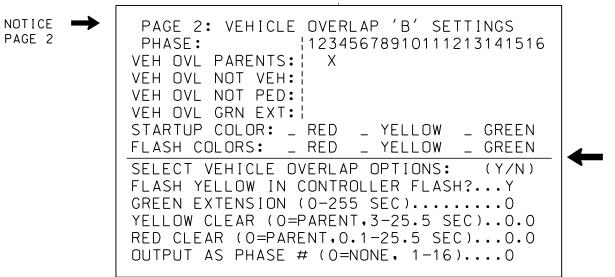
## OVERLAP PROGRAMMING DETAIL FOR ALTERNATE PHASING

PROJECT REFERENCE NO. SHEET NO. R-2577A Sig. 9.2

#### (program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS). PRESS 'NEXT' TO ADVANCE TO PAGE 2.





PRESS '+'



#### PRESS '+' TWO TIMES

PRESS '+' THREE TIMES

PAGE 1: VEHICLE OVERLAP 'G' SETTINGS 12345678910111213141516 VEH OVL PARENTS: X VEH OVL NOT VEH: | VEH OVL NOT PED: | VEH OVL GRN EXT: STARTUP COLOR: \_ RED \_ YELLOW \_ GREEN FLASH COLORS: \_ RED \_ YELLOW \_ GREEN SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?...N GREEN EXTENSION (0-255 SEC)..... YELLOW CLEAR (O=PARENT,3-25.5 SEC)..0.0 RED CLEAR (0=PARENT, 0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

OUTPUT AS PHASE # (0=NONE, 1-16)....0

OVERLAP G PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 09-0975T DESIGNED: February 2024 SEALED: February 12, 2024 REVISED:



8601 Six Forks Road Suite 700 | Raleigh, North Carolina 27615-296 NC License No. F-0112

Engineers | Construction Managers | Planners | Scientists www.rkk.com

New Installation - Temporary Design (TMP Phase III Step 5) Electrical Detail - Sheet 2 of 5

# ELECTRICAL AND PROGRAMMING DETAILS FOR: Prepared for the Offices of:

750 N.Greenfield Pkwy,Garner,NC 27529

US 158 WB (Reidsville Rd.)

SR 2396 (Old Belews Creek Rd.) Winston-Salem

PLAN DATE: February 2024 REVIEWED BY: DT Sears PREPARED BY: WP Erickson-Jones REVIEWED BY: REVISIONS INIT. DATE

FINAL UNLESS ALL SIGNATURES COMPLETED FESSION. 056142

DOCUMENT NOT CONSIDERED

Porter Jones SIG. INVENTORY NO. 09-0975T

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