ECONOLITE ASC/3-2070 LOGIC PROCESSOR PROGRAMMING DETAIL

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	(program controller as snown)
1. From M	ain Menu select 1. CONFIGURATION
2. From C	ONFIGURATION Submenu select 8. LOGIC PROCESSOR
3. From t	he LOGIC PROCESSOR Submenu select 2. LOGIC STATEMENTS
This log phase 7 (ic statement prevents the controller from serving at controller startup.
ENTER A "1 PROGRAM AS	" IN THE LP# FIELD, PRESS 'ENTER', AND SHOWN.
I ₽ #• 1	
IF PM	T PREEMPT ACTIVE 1 IS OFF AT STARTUP AND/OR WHEN NOT
THEN CT	R OMIT PHASE 7 ON
ELSE	
L	
1. From Ma	in Menu select 1. CONFIGURATION
2. From CO	INFIGURATION Submenu select 8, LOGIC PROCESSOR
S. From Th	E LUGIC PRUCESSUR SUDMENU SETECT [I. LUGIC STATEMENT CUNT
LOGIC STA	TEMENT CONTROL 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 F
LP 16-30	
LP 31-45	
LP 61-75	
LP 76-90	
	END PROGRAMMING
	ECONOLITE ASC/3-2070 OVERLAP PROGRAMMING DETAIL (program controller as shown)
	1. From Main Menu select 2. CONTROLLER
	2. From CONTROLLER Submerul select 2 VEHICLE OVERLAPS
	Togale Twice
	OVERLAP C
	Select TMG VEH OVLP [C] and 'NORMAL'
	TMG VEH OVLP[C] TYPE: NORMAL PHASES 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 INCLUDED X
	LAG GRN 0.0 YEL 0.0 RED 0.0
	END PROGRAMMING

<u>SEQUENCE PROGRAMMING DETAIL</u>	
(program controller as shown)	PED 3
1. From Main Menu select 1. CONFIGURATION	
2. From CONFIGURATION Submenu select 1. CONTROLLER SEQ	
3. From CONTROLLER SEQUENCE Submenu select	1. From Main
1. PHASE RING SEQUENCE AND ASSIGNMENT	2. From DETEC
Move the cursor to the SEQUENCE COMMANDS field, toggle to select "C" mode, enter phases in desired sequence.	
CONTROLLER SEQUENCE [1] SEQUENCE COMMANDS . HW ALT SEQ ENA. NO 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 BC- C C C C C C C C C C C C C C C R1- 1 2 3 4 7	
R2-56 R3	1. From Main
R4	2. From CONFI
R1-R4=RING 1-4, DATA ENTRY, PHASES 1-16 BC=BARRIER CONTROL, VALUES; B,C B=CURRENT GROUP RING BARRIER C=COMPATIBILITY PROGRAMMED BY MAIN MENU 1-1-2	
END SEQUENCE AND ASSIGNMENT PROGRAMMING From Main Menu select 1. CONFIGURATION From CONFIGURATION Submenu select 1. CONTROLLER SEQ From CONTROLLER SEQUENCE Submenu select 2. PHASE COMPATIBI	ITY
Program phase compatibility as shown below to ensure phases 3 and 7 cannot run concurrently.	NOTICE PHASE 3 PED ASSIGNED TO LD SWITCH 16 ■
PHASE COMPATIBILITY	
6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 .	
13 14	
15.	Final Design Electrical Detail – Sheet 2 of 3
END COMPATIBILITY PROGRAMMING	Stantec Prepa
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