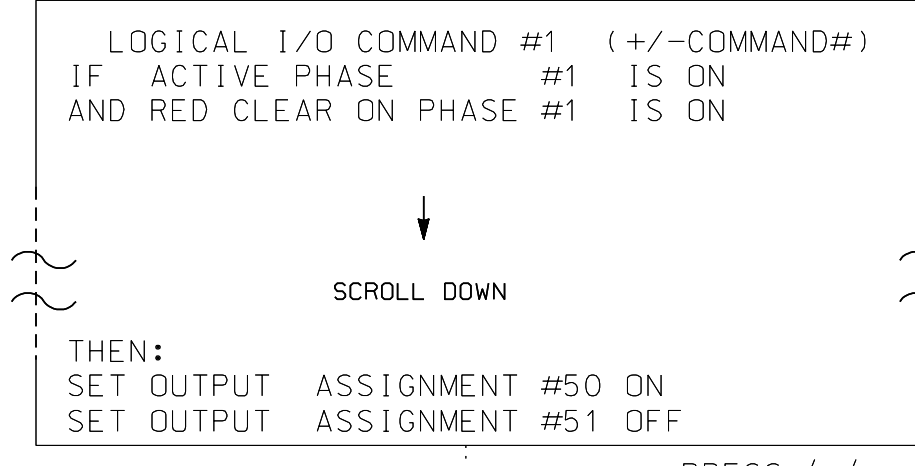


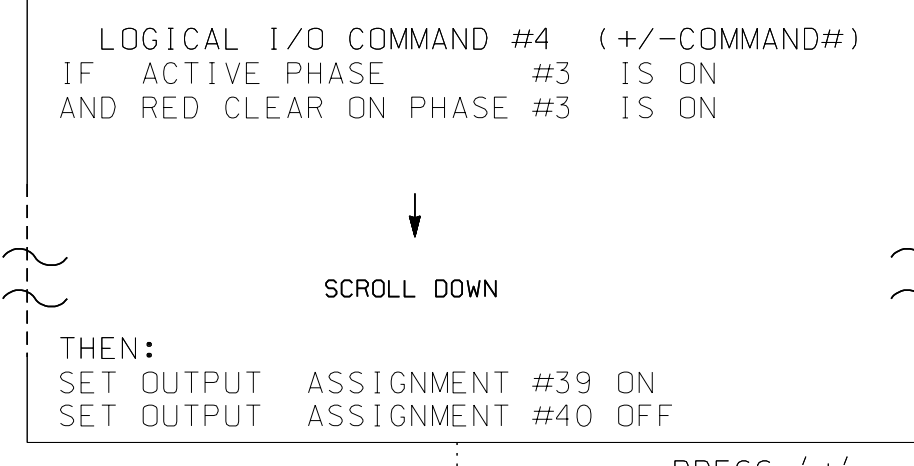
## LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

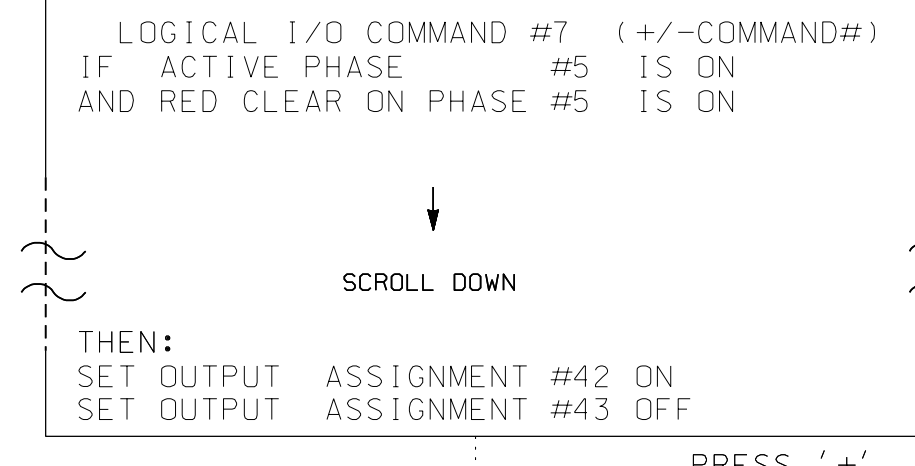
1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 AND 16.
2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



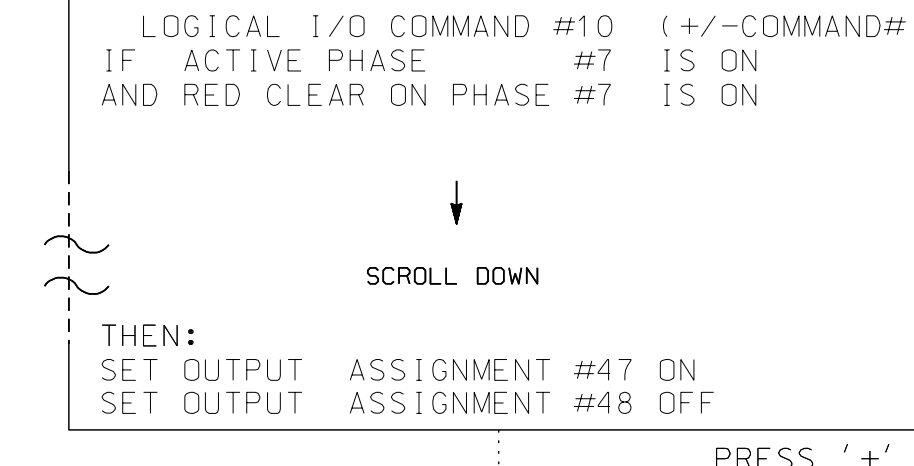
NOTE: LOGIC FOR PHASE 1 RED CLEAR WHEN TRANSITIONING FROM PHASE 1 TO PHASE 8 (HEAD 83).



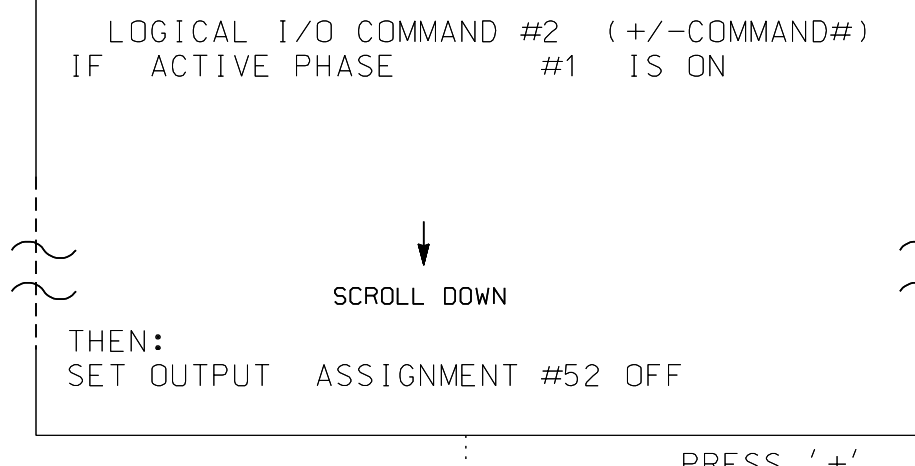
NOTE: LOGIC FOR PHASE 3 RED CLEAR WHEN TRANSITIONING FROM PHASE 5 TO PHASE 2 (HEAD 23).



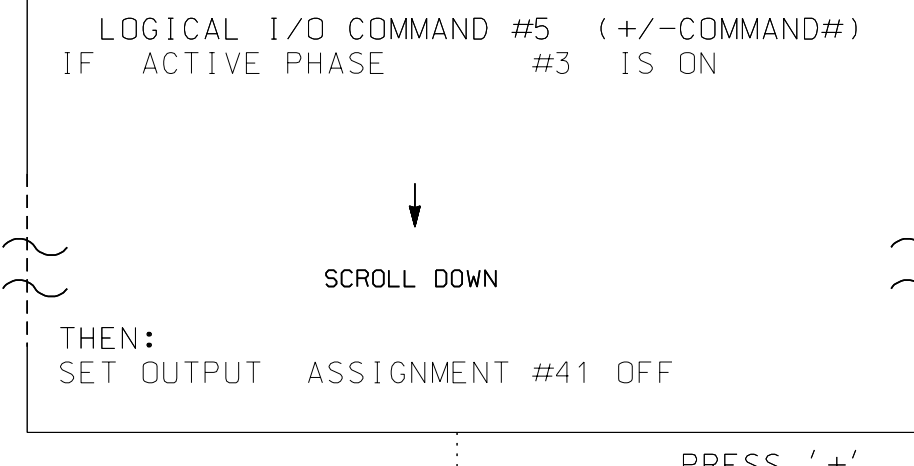
NOTE: LOGIC FOR PHASE 5 RED CLEAR WHEN TRANSITIONING FROM PHASE 5 TO PHASE 4 (HEAD 43).



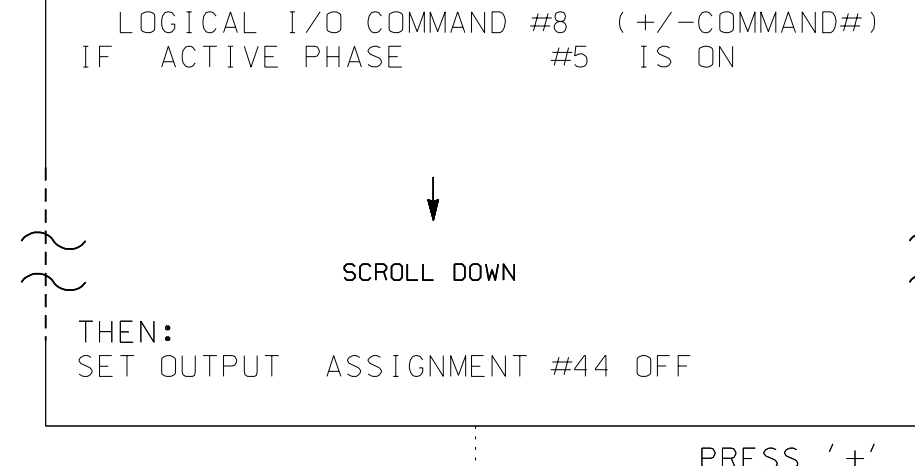
NOTE: LOGIC FOR PHASE 6 RED CLEAR WHEN TRANSITIONING FROM PHASE 7 TO PHASE 6 (HEAD 63).



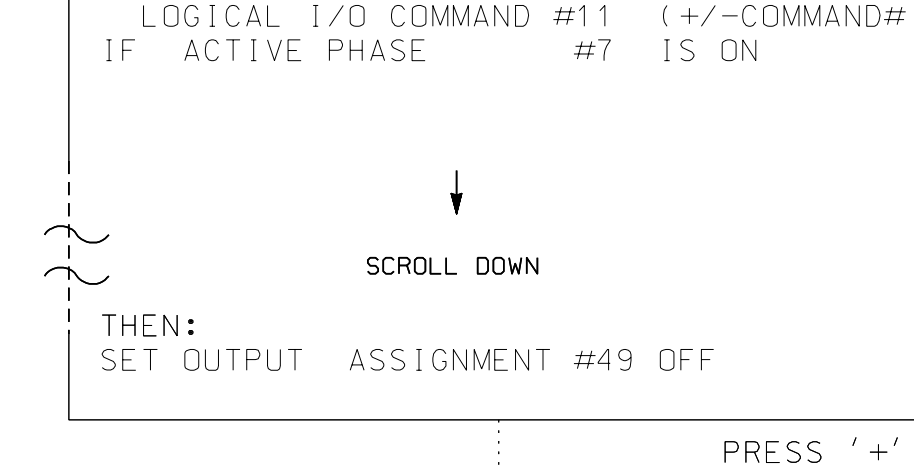
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 1 (HEAD 83).



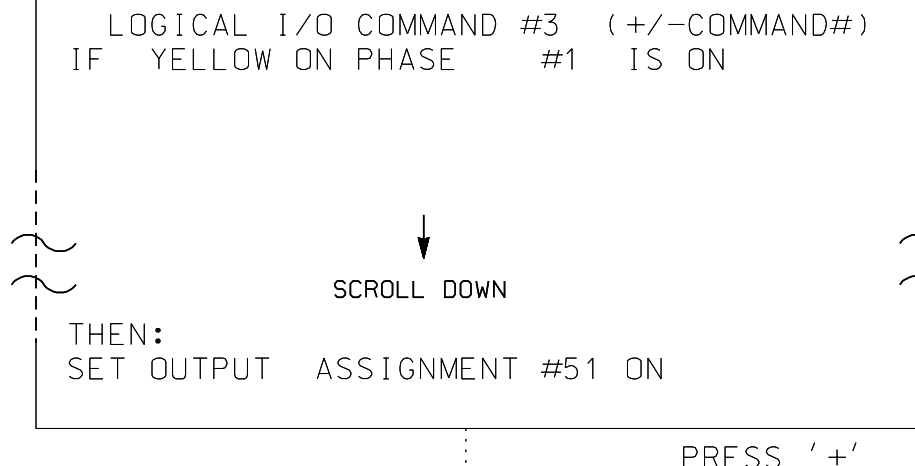
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 3 (HEAD 23).



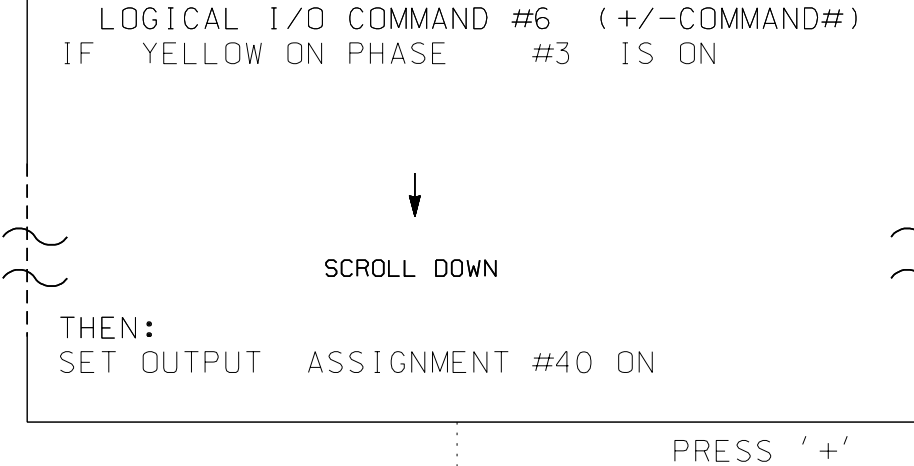
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 5 (HEAD 43).



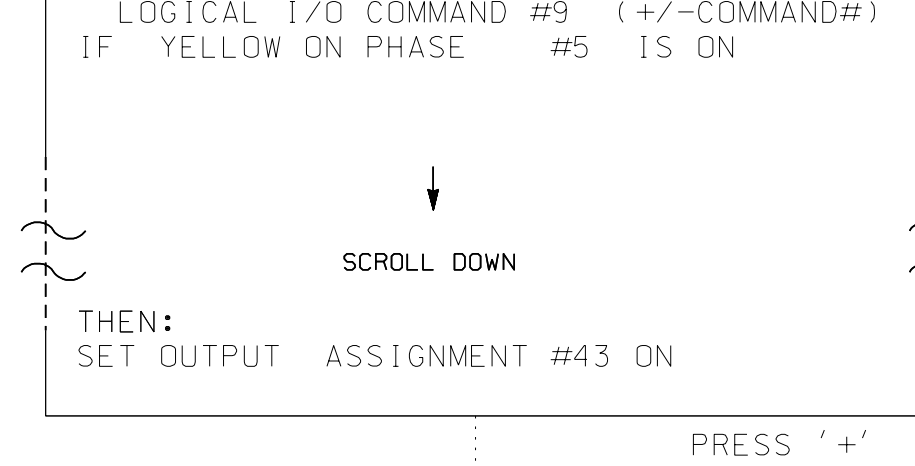
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 7 (HEAD 63).



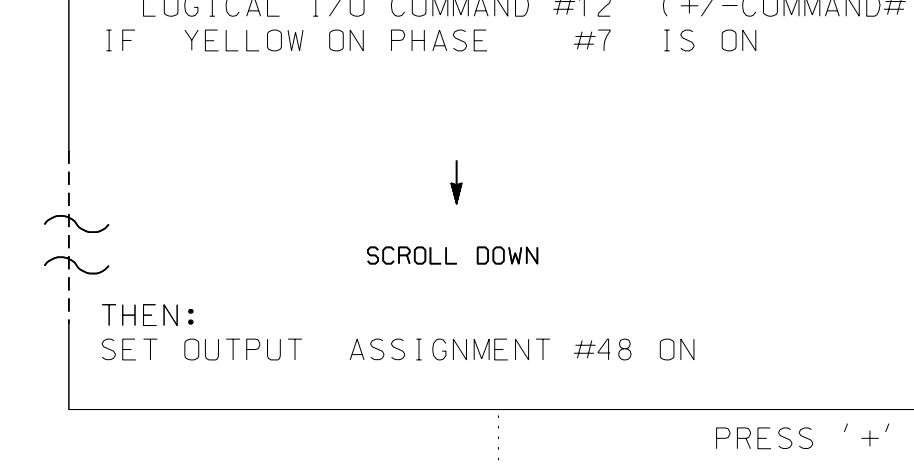
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 1 (HEAD 83).



NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 3 (HEAD 23).



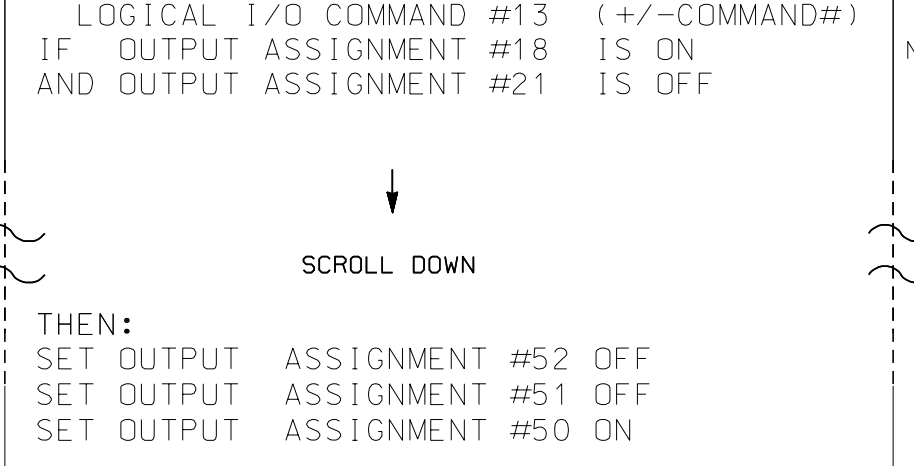
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 5 (HEAD 43).



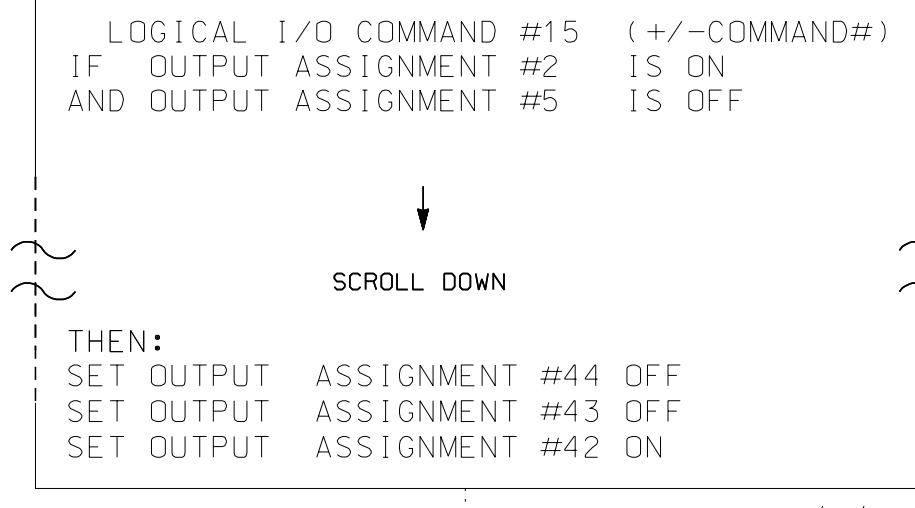
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 7 (HEAD 63).

**OUTPUT REFERENCE SCHEDULE**

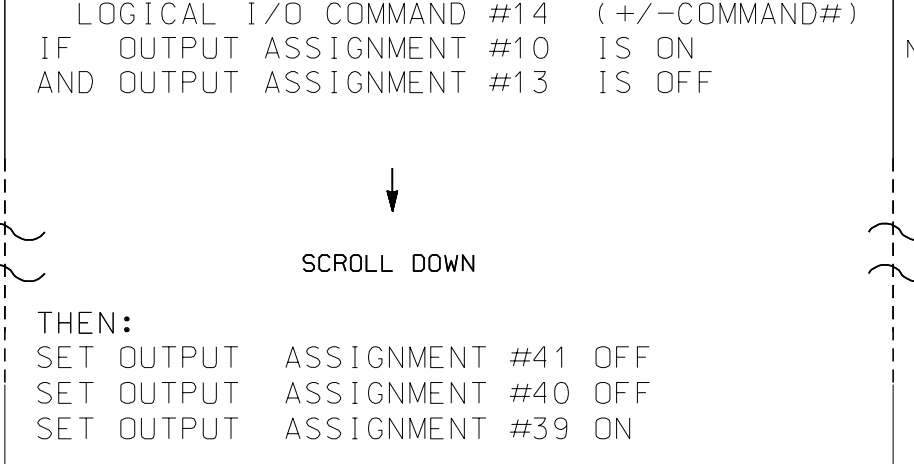
OUTPUT 2	=	PHASE 4 WALK
OUTPUT 5	=	PHASE 4 GREEN
OUTPUT 10	=	PHASE 2 WALK
OUTPUT 13	=	PHASE 2 GREEN
OUTPUT 18	=	PHASE 8 WALK
OUTPUT 21	=	PHASE 8 GREEN
OUTPUT 26	=	PHASE 6 WALK
OUTPUT 29	=	PHASE 6 GREEN
OUTPUT 39	=	Overlap D Red
OUTPUT 40	=	Overlap D Yellow
OUTPUT 41	=	Overlap D Green
OUTPUT 42	=	Overlap C Red
OUTPUT 43	=	Overlap C Yellow
OUTPUT 44	=	Overlap C Green
OUTPUT 47	=	Overlap B Red
OUTPUT 48	=	Overlap B Yellow
OUTPUT 49	=	Overlap B Green
OUTPUT 50	=	Overlap A Red
OUTPUT 51	=	Overlap A Yellow
OUTPUT 52	=	Overlap A Green



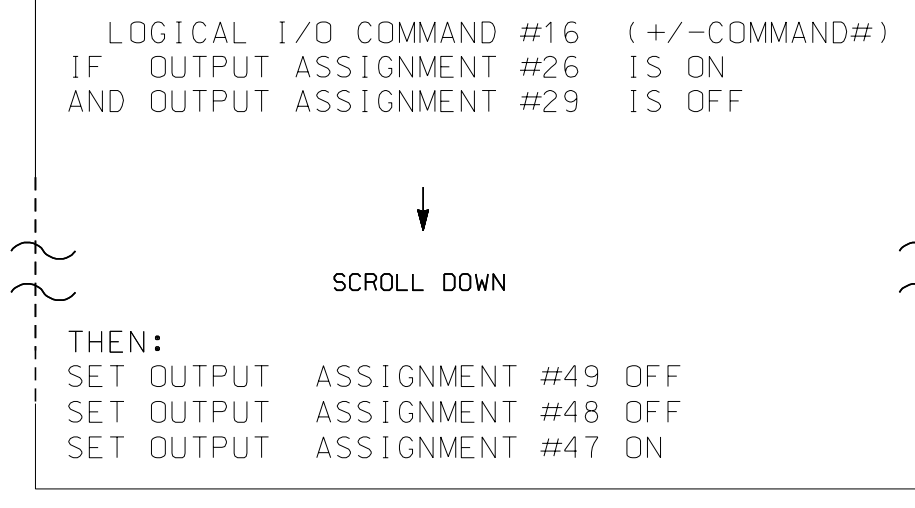
NOTE: LOGIC STATEMENT FOR ADVANCE WALK WITH FYA'S. TURN FYA HEAD 83 "OFF" DURING PED 8 ADVANCE WALK.



NOTE: LOGIC STATEMENT FOR ADVANCE WALK WITH FYA'S. TURN FYA HEAD 43 "OFF" DURING PED 4 ADVANCE WALK.



NOTE: LOGIC STATEMENT FOR ADVANCE WALK WITH FYA'S. TURN FYA HEAD 23 "OFF" DURING PED 2 ADVANCE WALK.

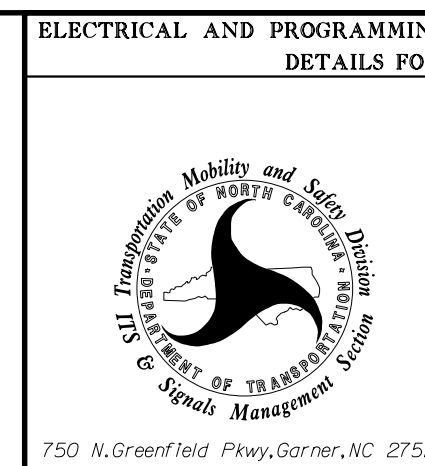
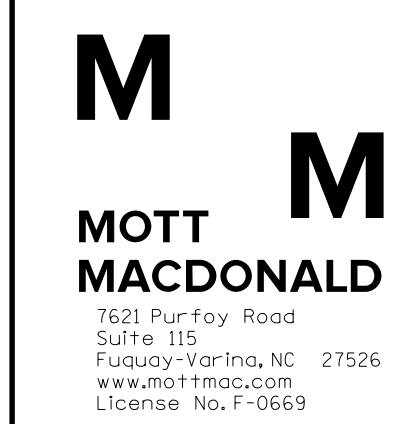


NOTE: LOGIC STATEMENT FOR ADVANCE WALK WITH FYA'S. TURN FYA HEAD 63 "OFF" DURING PED 6 ADVANCE WALK.

LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 09-0557T4  
DESIGNED: March 2023  
SEALED: April 25, 2023  
REVISED:

Electrical Detail - Temporary Design 4 - Sheet 4 of 5



ELECTRICAL AND PROGRAMMING DETAILS FOR:		SR 4000 (University Parkway) at SR 1672 (Hanes Mill Rd)	
Division 9	Forsyth County	Winston-Salem	
PLAN DATE: March 2023	REVIEWED BY: RW Thompson		
PREPARED BY: LD Stouchko	REVIEWED BY:		
REVISIONS	INIT.	DATE	

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



4/25/2023 G:\4308350\_DDC\_1\2\MFC-JL-2729\Foff\c451.dwg (s:\09-0557\4260\_375\_090557-20230425e4-14.dwg) User:R-151086227