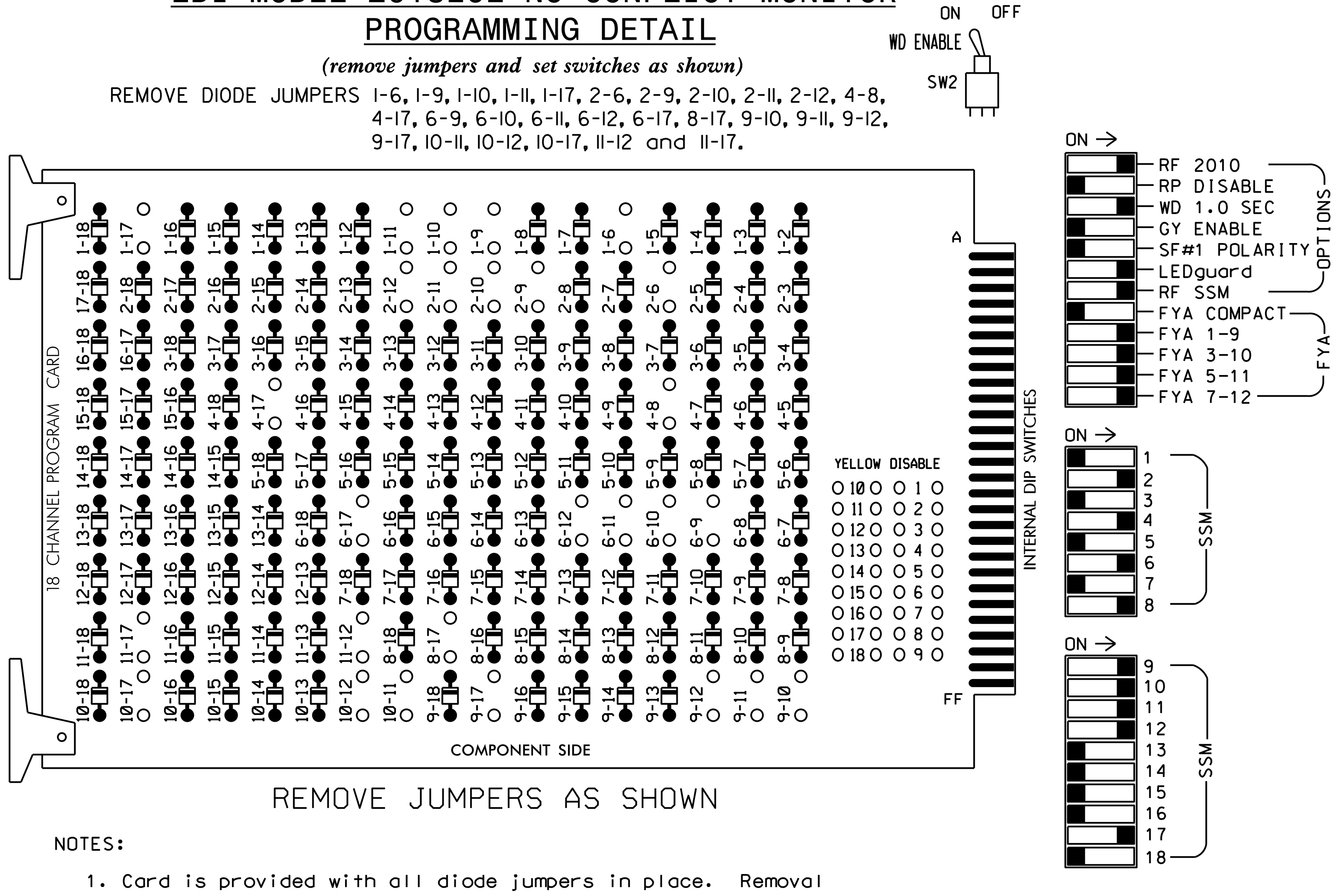
EDI MODEL 2018ECL-NC CONFLICT MONITOR PROGRAMMING DETAIL

(remove jumpers and set switches as shown)

REMOVE DIODE JUMPERS 1-6, 1-9, 1-10, 1-11, 1-17, 2-6, 2-9, 2-10, 2-11, 2-12, 4-8, 4-17, 6-9, 6-10, 6-11, 6-12, 6-17, 8-17, 9-10, 9-11, 9-12, 9-17, 10-11, 10-12, 10-17, 11-12 and 11-17.



REMOVE JUMPERS AS SHOWN

NOTES:

1. Card is provided with all diode jumpers in place. Removal of any jumper allows its channels to run concurrently.
2. Ensure jumpers SEL2-SEL5 and SEL9 are present on the monitor board.
3. Ensure that Red Enable is active at all times during normal operation.
4. Connect serial cable from conflict monitor to comm. port 1 of 2070 controller. Ensure conflict monitor communicates with 2070.

NOTES

1. To prevent "flash-conflict" problems, insert red flash program blocks for all unused vehicle load switches in the output file. The installer shall verify that signal heads flash in accordance with the Signal Plans.
2. Program phases 4 and 8 for Dual Entry.
3. Enable Simultaneous Gap-Out for all Phases.
4. Program phases 2 and 6 for Variable Initial and Gap Reduction.
5. Program phases 2 and 6 for Startup In Green.
6. Program phases 2 and 6 for Yellow Flash, and overlaps 1, 2 and 5 as Wag Overlaps.
7. If this signal will be managed by an ATMS software, enable controller and detector logging for all detectors used at this location.
8. The cabinet and controller are part of the US 70 Bus.-NC 42 (Clayton) D04-01_Clayton System.

EQUIPMENT INFORMATION

CONTROLLER..............2070
CABINET.................332 W/ AUX
SOFTWARE................ECONOLITE OASIS
CABINET MOUNT...........BASE
OUTPUT FILE POSITIONS...18 WITH AUX. OUTPUT FILE
LOAD SWITCHES USED......S1, S2, S5, S8, S11, AUX S1, AUX S2, AUX S3, AUX S4, AUX S5
PHASES USED.............1, 2, 4, 6, 8
OVERLAP "A".............1+2
OVERLAP "B".............6
OVERLAP "C".............6
OVERLAP "D".............2
OVERLAP "E".............1+8

SIGNAL HEAD HOOK-UP CHART

LOAD SWITCH NO.	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	AUX S1	AUX S2	AUX S3	AUX S4	AUX S5	AUX S6
CMU CHANNEL NO.	1	2	13	3	4	14	5	6	15	7	8	16	9	10	17	11	12	18
PHASE	1	2	2 PED	3	4	4 PED	5	6	6 PED	7	8	8 PED	OLA	OLB	OLE	OLC	OLD	SPARE
SIGNAL HEAD NO.	11★	22,23	NU	NU	41,42	NU	NU	61,62	NU	NU	81,82	NU	11★	63★	83★	21★	24★	NU
RED		128			101			134			107			A124	A111		A101	
YELLOW	✻	129			102			135			108							
GREEN		130			103			136			109							
RED ARROW													A121			A114		
YELLOW ARROW													A122	A125	A112	A115	A102	
FLASHING YELLOW ARROW													A123	A126	A113	A116	A103	
GREEN ARROW	127																	

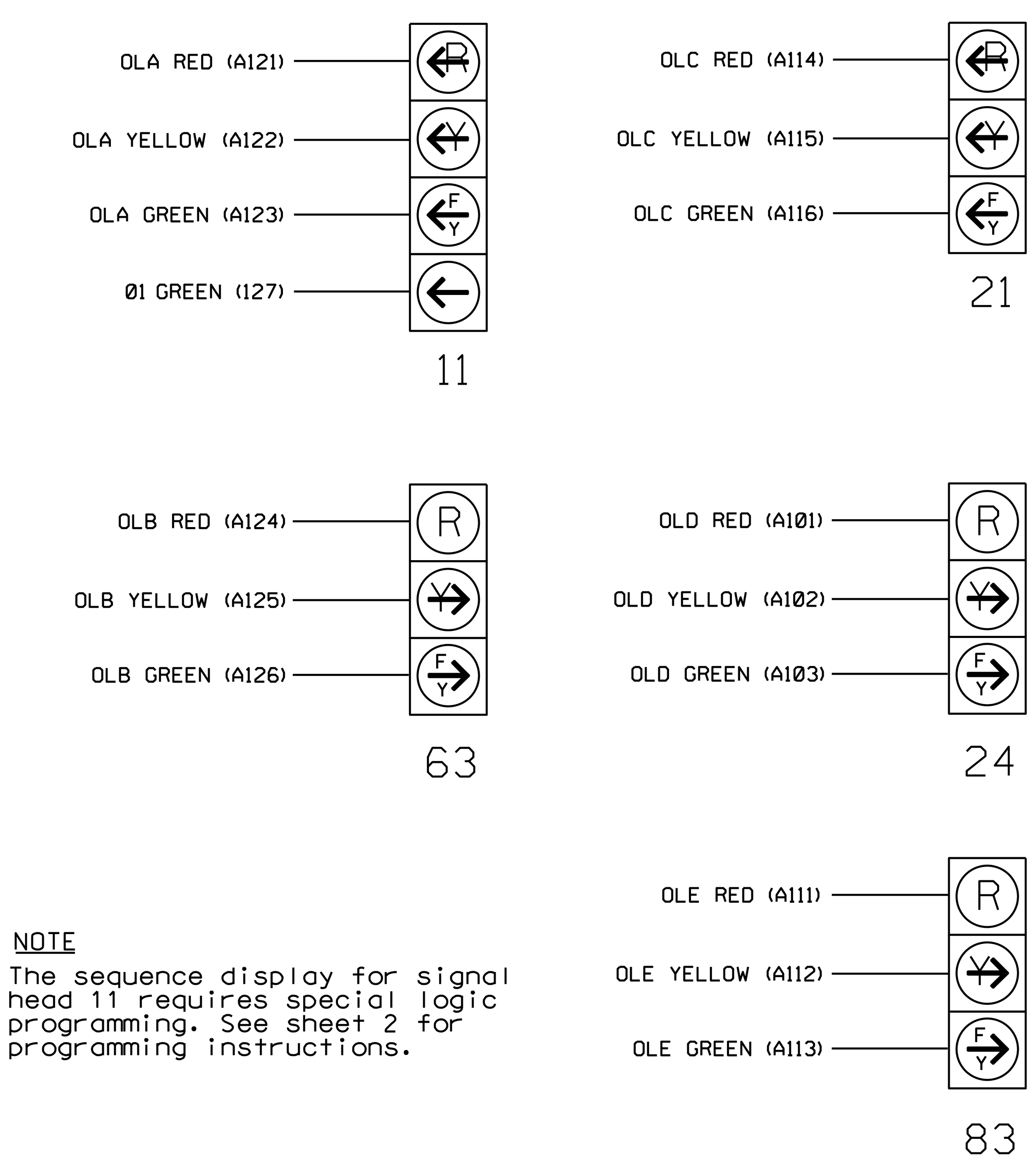
NU = Not Used

✻ Denotes install load resistor. See load resistor installation detail this sheet.

★ See pictorial of head wiring in detail this sheet.

FYA SIGNAL WIRING DETAIL

(wire signal heads as shown)



NOTE

The sequence display for signal head 11 requires special logic programming. See sheet 2 for programming instructions.

INPUT FILE POSITION LAYOUT

(front view)

		1	2	3	4	5	6	7	8	9	10	11	12	13	14
FILE "I"	U	Ø1 1A	Ø2 2A	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	Ø4 4A	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	FS DC ISOLATOR
	L	NOT USED	Ø2 2B				NOT USED								ST DC ISOLATOR
FILE "J"	U	SLOT EMPTY	Ø6 6A	SLOT EMPTY	WIRED INPUT ⊗	SLOT EMPTY	Ø8 8A	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY
	L		NOT USED				Ø1 1B								

EX.: 1A, 2A, ETC. = LOOP NO.'S

FS = FLASH SENSE
ST = STOP TIME

⊗ Wired Input - Do not populate slot with detector card

INPUT FILE CONNECTION & PROGRAMMING CHART

LOOP NO.	LOOP TERMINAL	INPUT FILE POS.	PIN NO.	INPUT ASSIGNMENT NO.	DETECTOR NO.	NEMA PHASE	CALL	EXTEND	FULL TIME DELAY	STRETCH TIME	DELAY TIME
1A[1]	TB2-1,2	I1U	56	18	1	1	Y	Y			15
	-	J4U	48	10	26	6	Y	Y	Y		3
1B	TB5-11,12	J6L	46	8	18	1	Y	Y			15
2A	TB2-5,6	I2U	39	1	2	2	Y	Y			
2B	TB2-7,8	I2L	43	5	12	2	Y	Y	Y		3
4A	TB4-9,10	I6U	41	3	4	4	Y	Y			3
6A	TB3-5,6	J2U	40	2	6	6	Y	Y			
8A	TB5-9,10	J6U	42	4	8	8	Y	Y			3

[1] Add jumper from I1-W to J4-W, on rear of input file.

INPUT FILE POSITION LEGEND: J2L

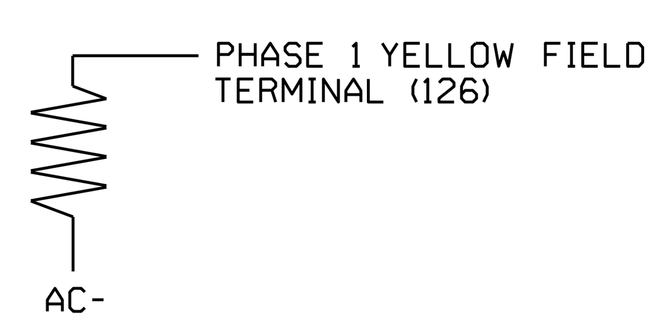
FILE J
SLOT 2
LOWER

LOAD RESISTOR INSTALLATION DETAIL

(install resistor as shown below)

ACCEPTABLE VALUES

VALUE (ohms)	WATTAGE
1.5K - 1.9K	25W (min)
2.0K - 3.0K	10W (min)



THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 04-1449
DESIGNED: January 2022
SEALED: 3/29/2022
REVISED: N/A

Electrical Detail - Sheet 1 of 2

ELECTRICAL AND PROGRAMMING DETAILS FOR:

SR 1560 (-L-)
at
SR 1563 (-Y1-) /
Future Road By Others

Division 4 Johnston County Clayton

PLAN DATE: March 2022 REVIEWED BY:
PREPARED BY: Zarrar Zafar REVIEWED BY:

REVISIONS INIT. DATE

Prepared in the Offices of:
Transportation Mobility and Safety Division, Signals Management Section
750 N.Greenfield Pkwy,Garner,NC 27529

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED

SEAL
NORTH CAROLINA PROFESSIONAL SEAL 031001 ENGINEER D. TODD JOYCE

DocuSigned by: D. Todd Joyce 03/30/2022
DATE

SIG. INVENTORY NO. 04-1449

30-MAR-2022 15:42
zzafar