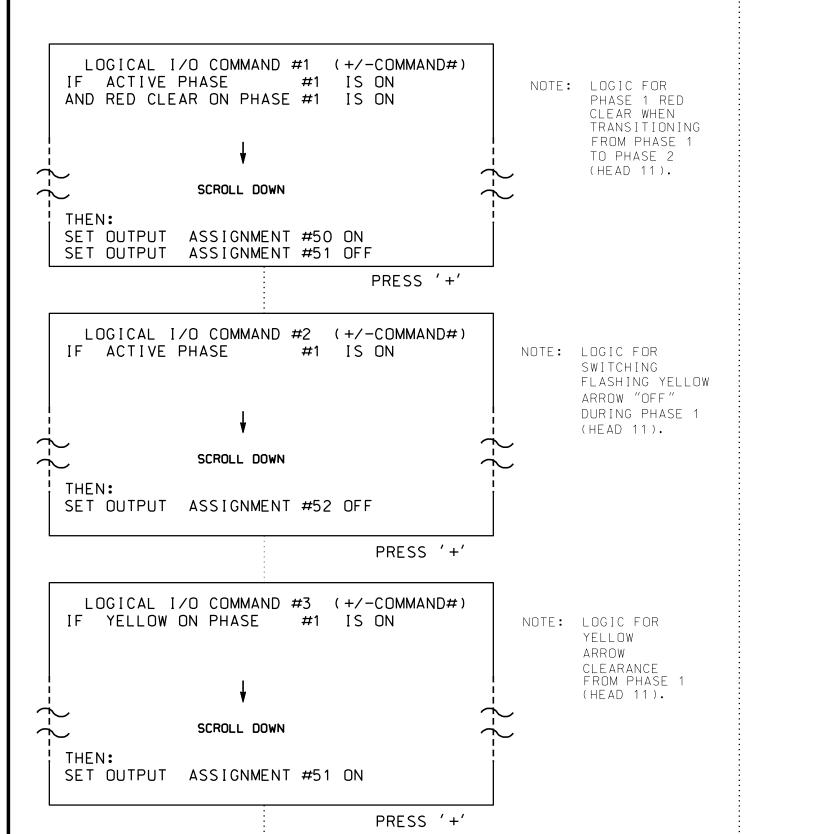
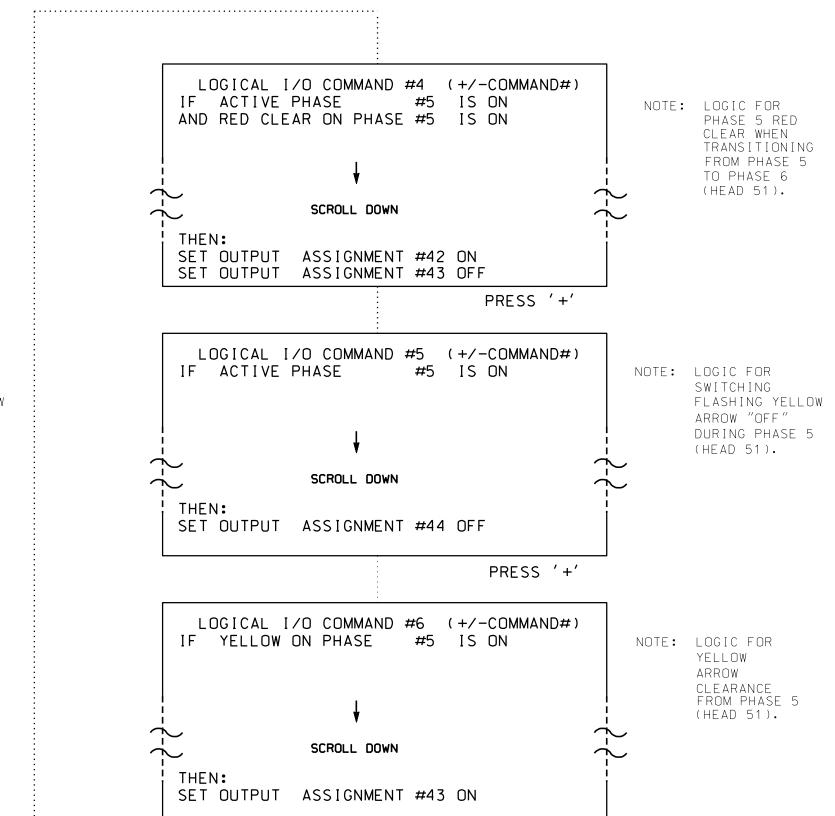
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5 AND 6.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).





LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OUTPUT REFERENCE SCHEDULE

OUTPUT 42 = Overlap C Red OUTPUT 43 = Overlap C Yellow OUTPUT 44 = Overlap C Green OUTPUT 50 = Overlap A Red OUTPUT 51 = Overlap A Yellow OUTPUT 52 = Overlap A Green

> THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 03-1152 DESIGNED: Nov 2021 SEALED: 11/08/2021 REVISED: N/A

ALTERNATE PHASING ACTIVATION DETAIL

TO RUN ALT. PHASING DURING <u>COORDINATION</u> - SELECT ALL PAGE CHANGES (AS SHOWN BELOW) WITHIN COORDINATION PLAN PROGRAMMING.

TO RUN ALT. PHASING DURING <u>Free run</u> — Program page Changes (Shown Below) in Separate time of DAY EVENTS. IF PAGE 1 IS USED, NO EVENT PROGRAMMING IS NECESSARY FOR THAT PARTICULAR PAGE.

| PHASING | INPUTS PAGE | OVERLAPS PAGE |
|---------------------------------------|-------------|---------------|
| ACTIVE PAGES REQUIRED TO RUN DEFAULT | PHASING 1 | 1 |
| ACTIVE PAGES REQUIRED TO RUN ALTERNAT | E PHASING 2 | 2 |

NOTE: PAGES NOT SHOWN (i.e. sequence, phase control, etc.) SHOULD REMAIN AS '1', OR AS DEFINED BY TIMING ENGINEER.

IMPORTANT: IF ALT. PHASING IS USED DURING FREE RUN AND COORDINATION, DO NOT OPERATE TIME OF DAY PAGE CHANGE EVENTS CONCURRENTLY WITH COORDINATION PLAN EVENTS IN THE EVENT SCHEDULER. (EX. FREE RUN PAGE CHANGE EVENT SHOULD END BEFORE COORDINATION PLAN EVENT STARTS AND VICE-VERSA).

ALTERNATE PHASING PAGE CHANGE SUMMARY

THE FOLLOWING IS A SUMMARY OF WHAT TAKES PLACE WHEN THESE OVERLAP/INPUT PAGE CHANGES ACTIVATE TO CALL THE "ALTERNATE PHASING":

OVERLAPS PAGE 2: Modifies overlap parent phases for heads 11 and 51 to

run protected turns only.

INPUTS PAGE 2: Disables phase 6 call on loop 1A

and reduces delay time for phase 1 call on loop 1A to 0 seconds.

Disables phase 2 call on loop 5A and reduces delay time for phase 5 call on loop 5A to 0 seconds.

Electrical Detail Sheet 2 of 5

ELECTRICAL AND PROGRAMMING DETAILS FOR:

Drysdale Drive



REVISIONS

PREPARED BY: A. Andrews | RKA PROJ. NO.: 19258 (040) INIT. DATE

William J. Hamilton 11/08/202 SIG. INVENTORY NO. 03-1152

DOCUMENT NOT CONSIDERED

FINAL UNLESS ALL SIGNATURES COMPLETED





750 N.Greenfield Pkwy.Garner.NC 27529