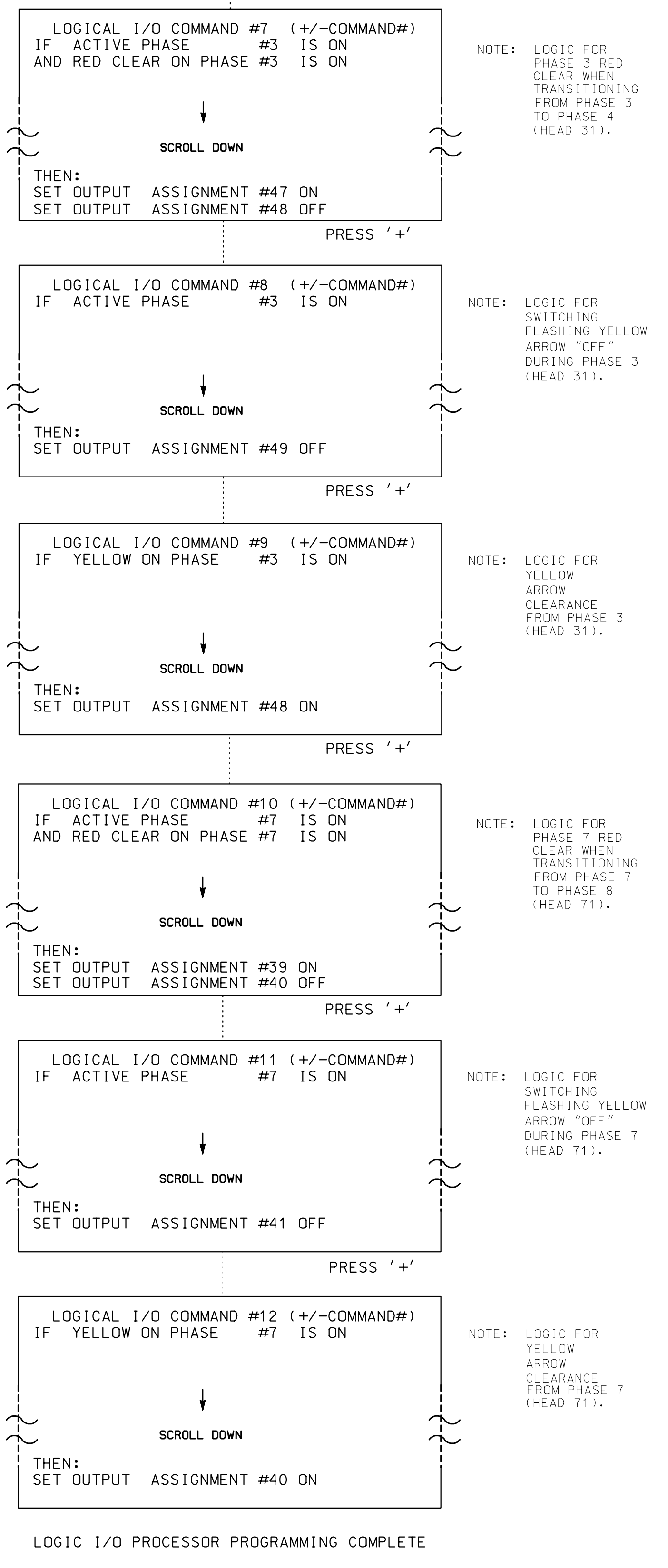
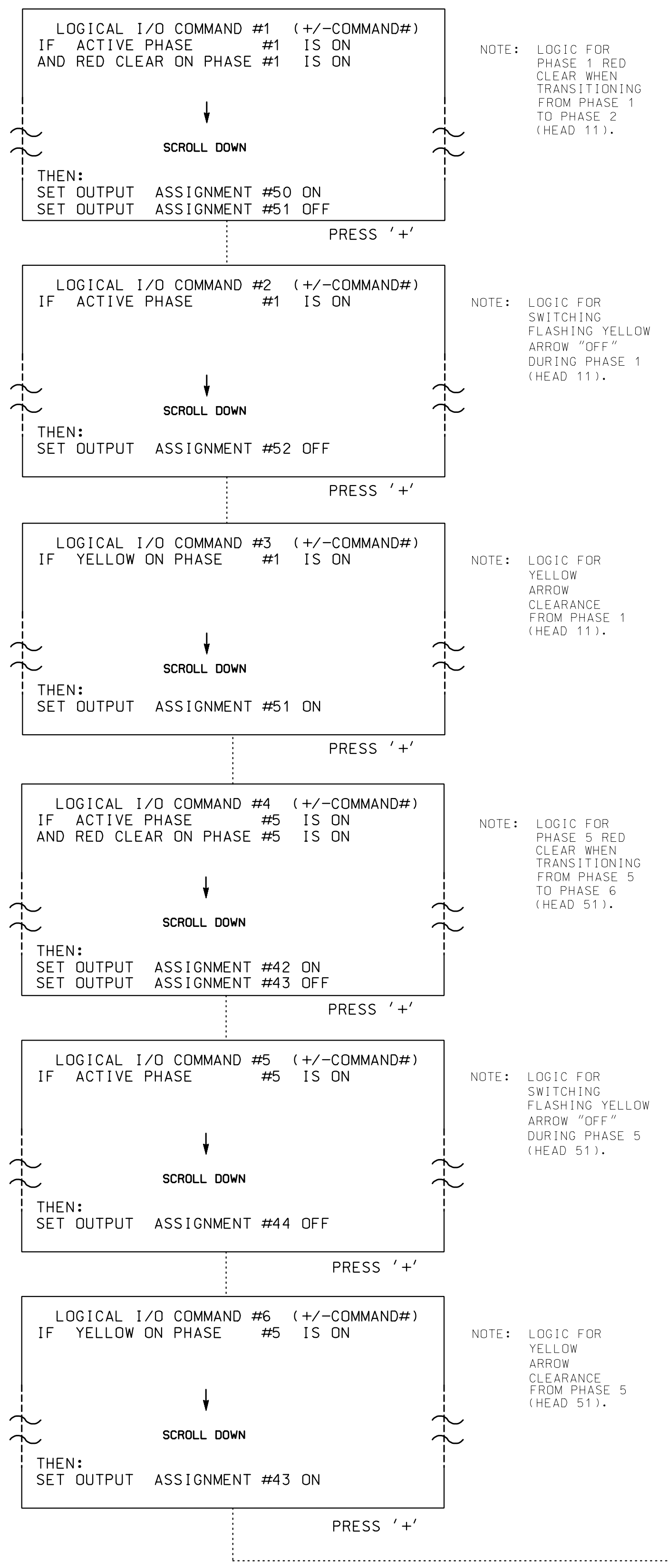


LOGICAL I/O PROCESSOR PROGRAMMING DETAIL  
TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

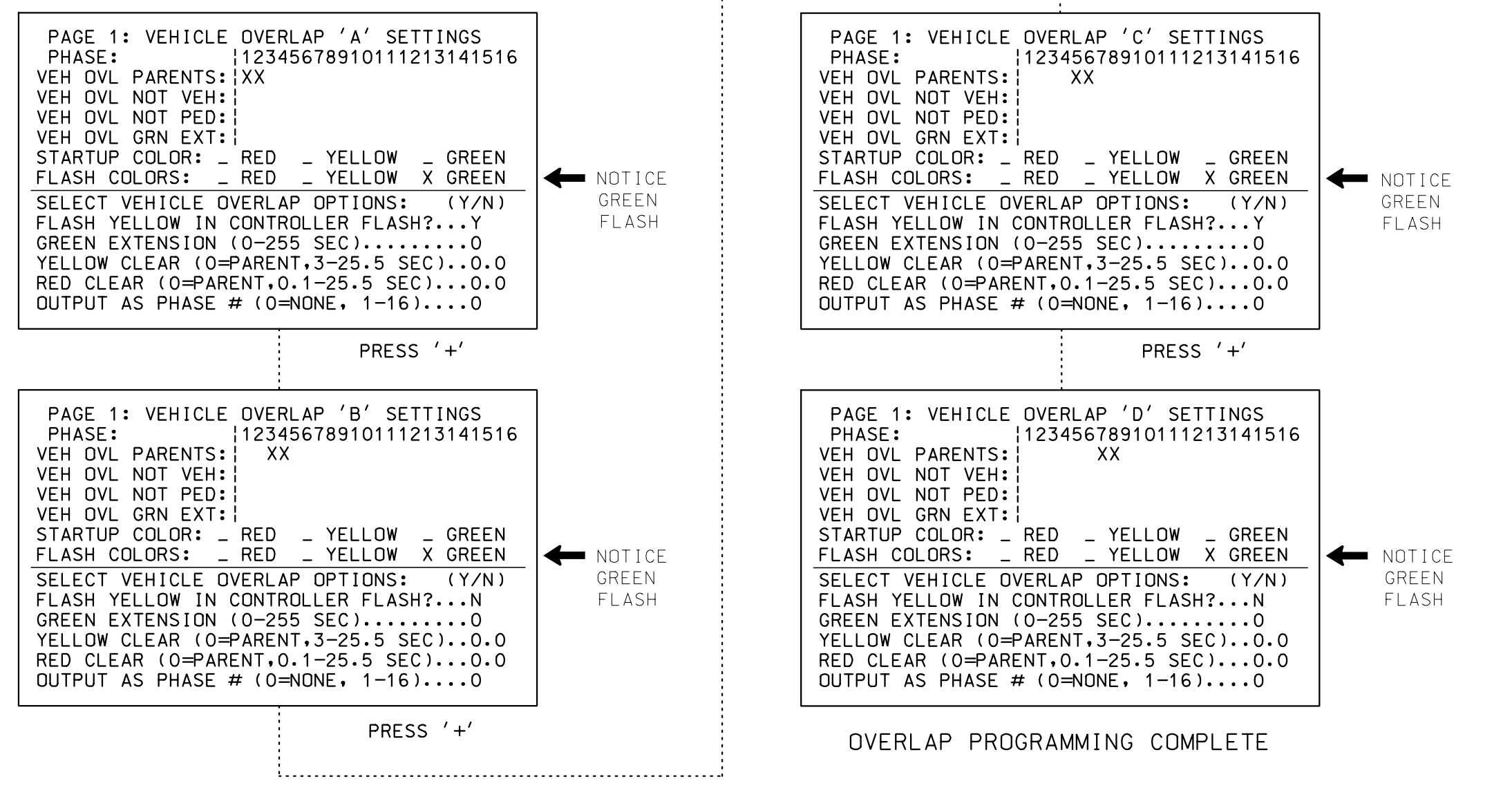
- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, AND 12.
2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OVERLAP PROGRAMMING DETAIL FOR DEFAULT PHASING  
(program controller as shown below)

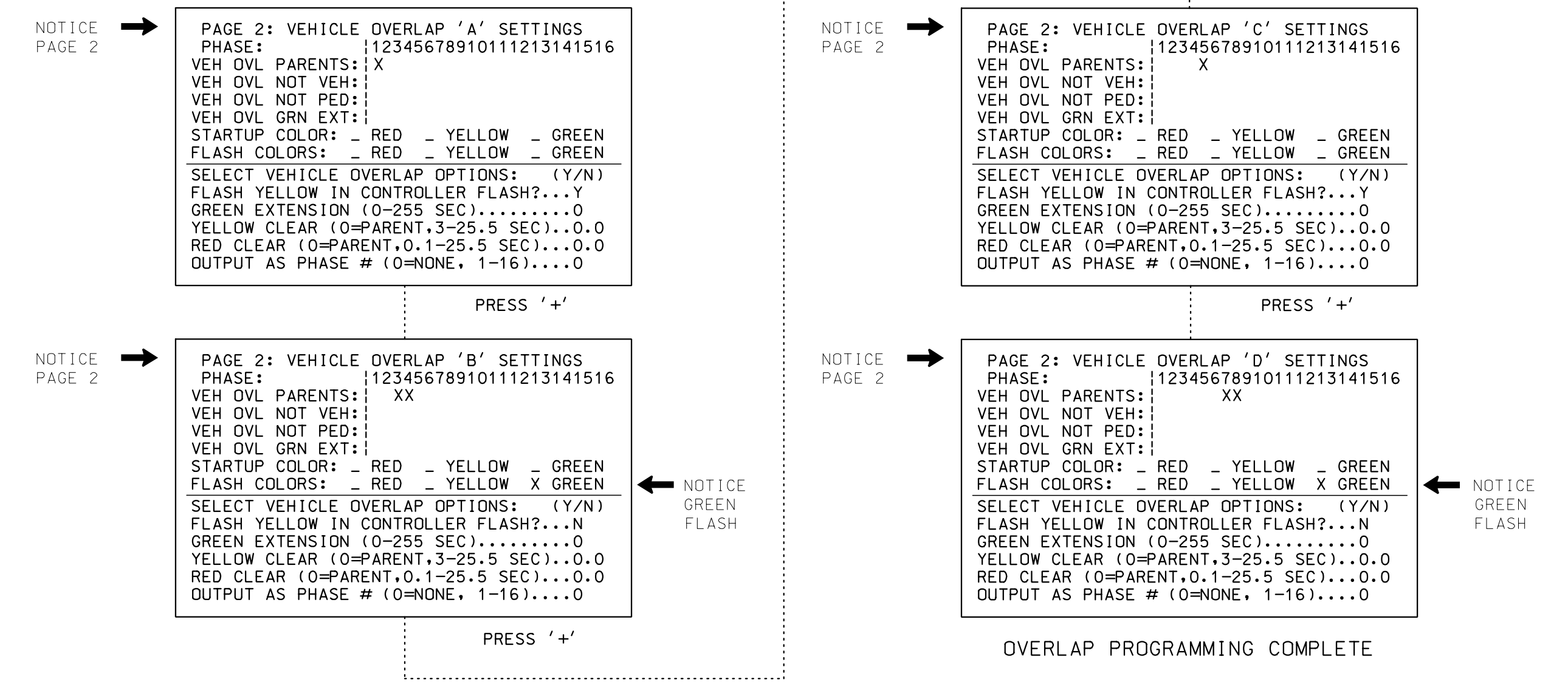
FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).



OVERLAP PROGRAMMING COMPLETE

OVERLAP PROGRAMMING DETAIL FOR ALTERNATE PHASING  
(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS), PRESS 'NEXT' TO ADVANCE TO PAGE 2.



OVERLAP PROGRAMMING COMPLETE

OUTPUT REFERENCE SCHEDULE
USE TO INTERPRET LOGIC PROCESSOR
OUTPUT 39 = Overlap D Red
OUTPUT 40 = Overlap D Yellow
OUTPUT 41 = Overlap D Green
OUTPUT 42 = Overlap C Red
OUTPUT 43 = Overlap C Yellow
OUTPUT 44 = Overlap C Green
OUTPUT 47 = Overlap B Red
OUTPUT 48 = Overlap B Yellow
OUTPUT 49 = Overlap B Green
OUTPUT 50 = Overlap A Red
OUTPUT 51 = Overlap A Yellow
OUTPUT 52 = Overlap A Green

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 09-0991
DESIGNED: NOVEMBER 2021
SEALED: 12/3/2021
REVISED: N/A

Final Design
Electrical Detail - Sheet 2 of 5

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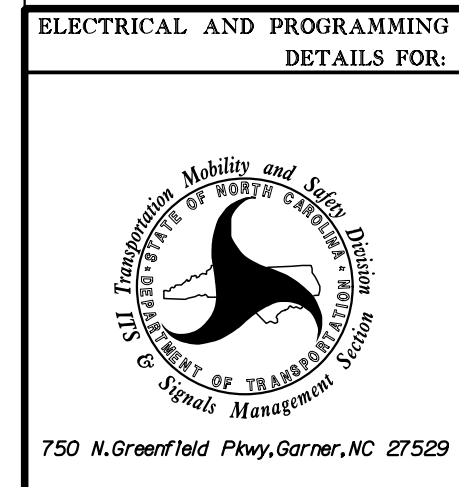


Table with columns: REVISIONS, INIT., DATE. Includes revision history for the document.

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED
SEAL
NORTH CAROLINA PROFESSIONAL ENGINEER SEAL
ZHAOLONG TENG
12/3/2021

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