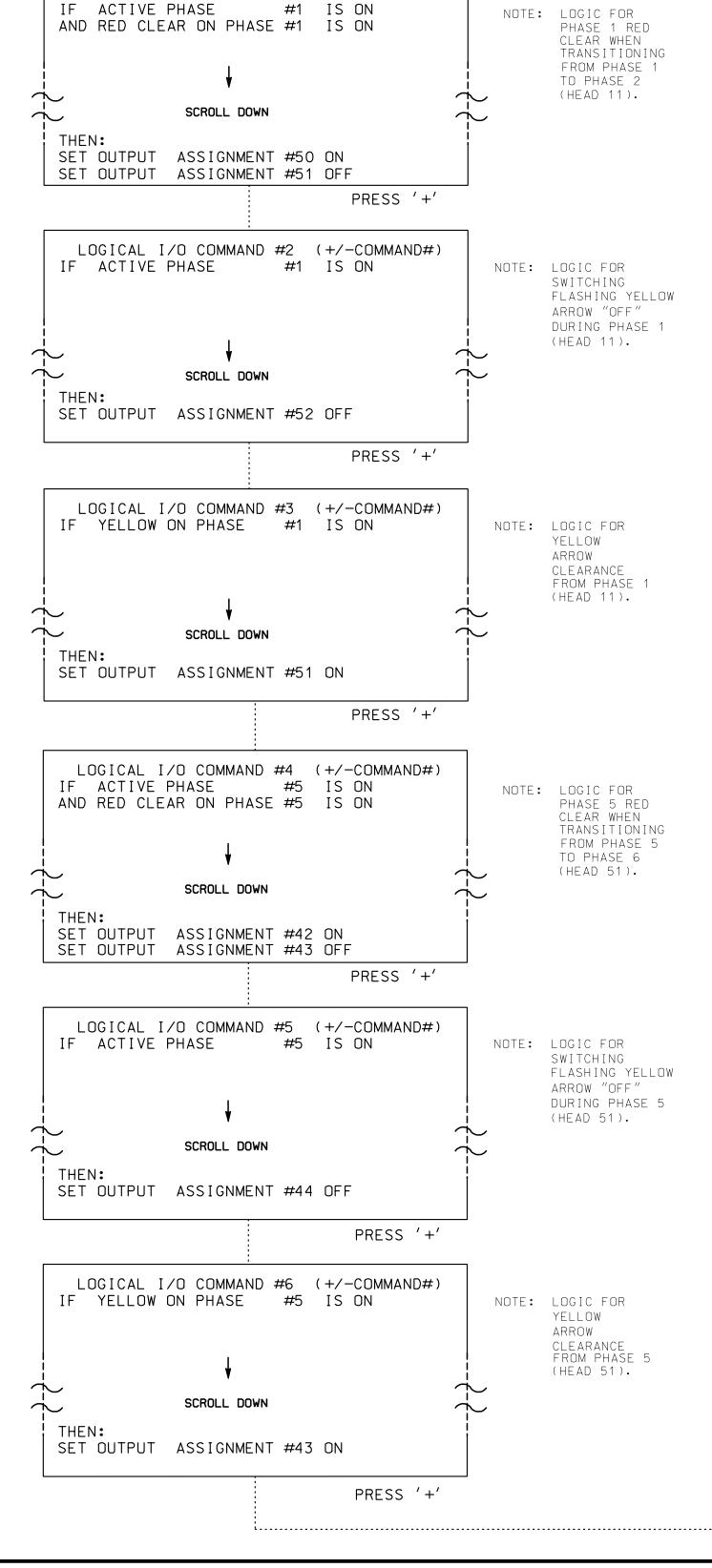
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

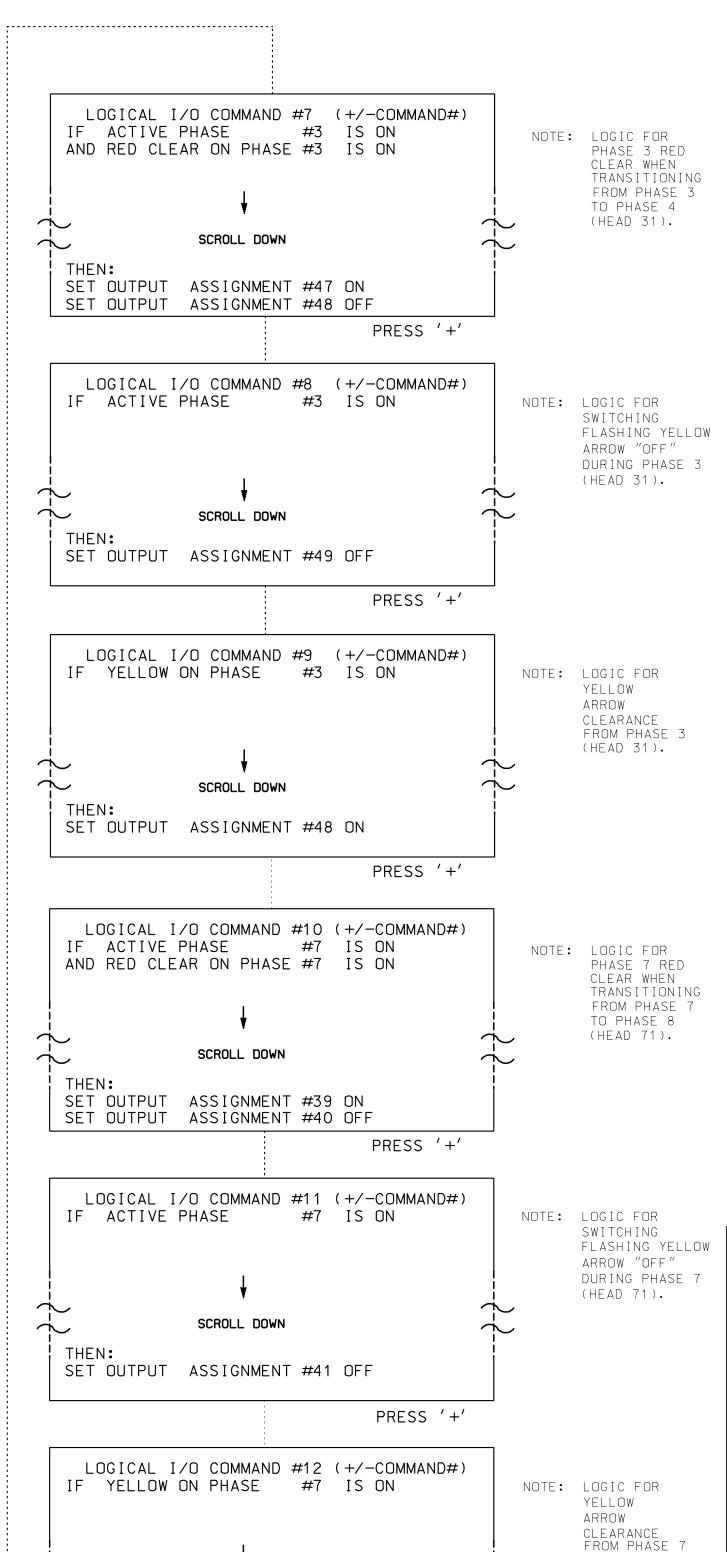
(program controller as shown below)

1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, AND 12.

2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).

LOGICAL I/O COMMAND #1 (+/-COMMAND#)





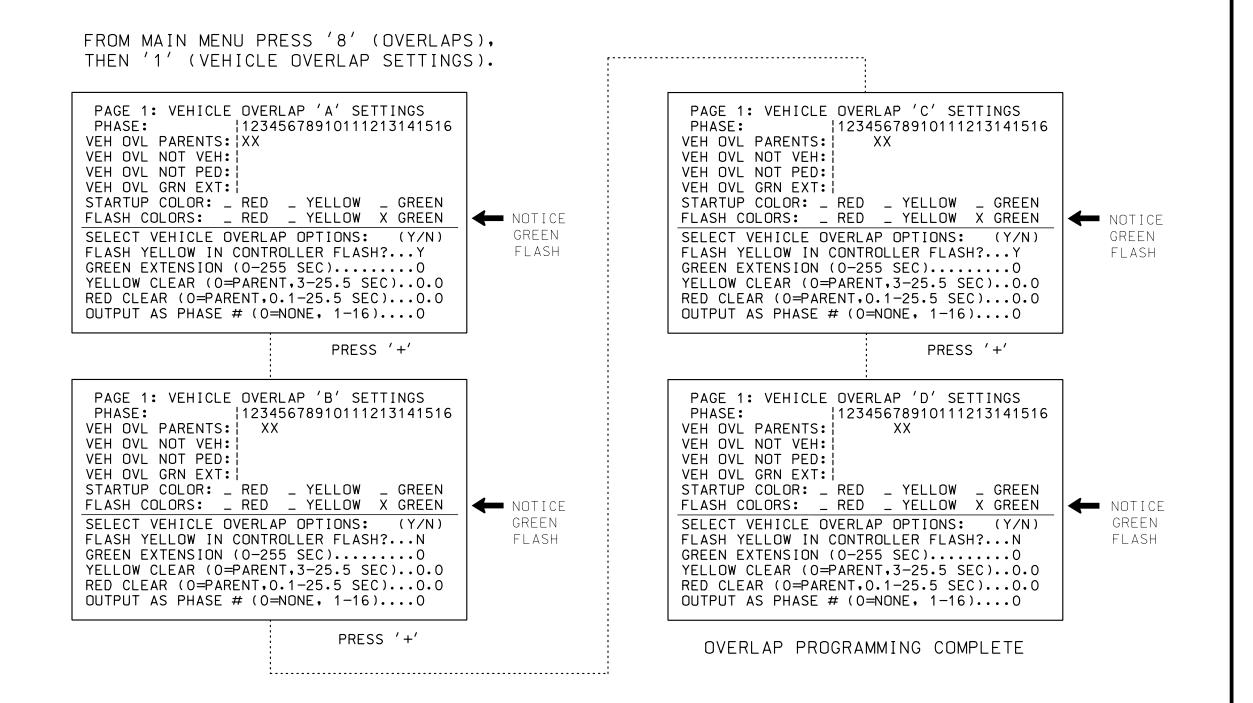
SCROLL DOWN

LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

SET OUTPUT ASSIGNMENT #40 ON

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

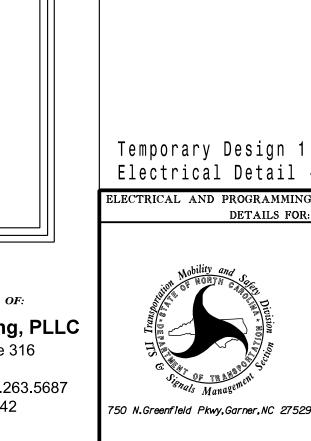


FLASHER CIRCUIT MODIFICATION DETAIL

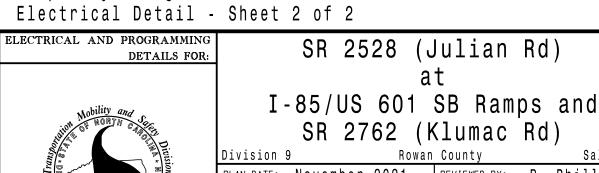
IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

- 1. ON REAR OF PDA REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
- 2. ON REAR OF PDA REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
- 3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.



THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: Ø9-Ø991T1 DESIGNED: NOVEMBER 2Ø21 SEALED: 12/3/2021 REVISED: N/A



I-85/US 601 SB Ramps and SR 2762 (Klumac Rd)

Division 9 Rowan County Salisbury

PLAN DATE: November 2021 REVIEWED BY: B. Phillips

PREPARED BY: Z. "Gavin" Teng REVIEWED BY:

REVISIONS INIT. DATE

DOCUMENT NOT CONSIDERED

FINAL UNLESS ALL

SIGNATURES COMPLETED

\$\$\$\$\$\Z\IME\$\$\$\$\$

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OUTPUT REFERENCE SCHEDULE

USE TO INTERPRET LOGIC PROCESSOR

OUTPUT 40 = Overlap D Yellow

OUTPUT 43 = Overlap C Yellow

OUTPUT 44 = Overlap C Green

OUTPUT 49 = Overlap B Green

OUTPUT 51 = Overlap A Yellow

OUTPUT 52 = Overlap A Green

(HEAD 71).

OUTPUT 50 = Overlap A Red

OUTPUT 47 = Overlap B Red OUTPUT 48 = Overlap B Yellow

OUTPUT 41 = Overlap D Green

OUTPUT 39 = Overlap D Red

OUTPUT 42 = Overlap C Red