

## LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS), SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, AND 12.
2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).

```

LOGICAL I/O COMMAND #1 (+/-COMMAND#)
IF ACTIVE PHASE #1 IS ON
AND RED CLEAR ON PHASE #1 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #50 ON
SET OUTPUT ASSIGNMENT #51 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR PHASE 1 RED CLEAR WHEN TRANSITIONING FROM PHASE 1 TO PHASE 2 (HEAD 11).

```

LOGICAL I/O COMMAND #2 (+/-COMMAND#)
IF ACTIVE PHASE #1 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #52 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 1 (HEAD 11).

```

LOGICAL I/O COMMAND #3 (+/-COMMAND#)
IF YELLOW ON PHASE #1 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #51 ON
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 1 (HEAD 11).

```

LOGICAL I/O COMMAND #4 (+/-COMMAND#)
IF ACTIVE PHASE #5 IS ON
AND RED CLEAR ON PHASE #5 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #42 ON
SET OUTPUT ASSIGNMENT #43 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR PHASE 5 RED CLEAR WHEN TRANSITIONING FROM PHASE 5 TO PHASE 6 (HEAD 51).

```

LOGICAL I/O COMMAND #5 (+/-COMMAND#)
IF ACTIVE PHASE #5 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #44 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 5 (HEAD 51).

```

LOGICAL I/O COMMAND #6 (+/-COMMAND#)
IF YELLOW ON PHASE #5 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #43 ON
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 5 (HEAD 51).

```

LOGICAL I/O COMMAND #7 (+/-COMMAND#)
IF ACTIVE PHASE #3 IS ON
AND RED CLEAR ON PHASE #3 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #47 ON
SET OUTPUT ASSIGNMENT #48 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR PHASE 3 RED CLEAR WHEN TRANSITIONING FROM PHASE 3 TO PHASE 4 (HEAD 31).

```

LOGICAL I/O COMMAND #8 (+/-COMMAND#)
IF ACTIVE PHASE #3 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #49 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 3 (HEAD 31).

```

LOGICAL I/O COMMAND #9 (+/-COMMAND#)
IF YELLOW ON PHASE #3 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #48 ON
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 3 (HEAD 31).

```

LOGICAL I/O COMMAND #10 (+/-COMMAND#)
IF ACTIVE PHASE #7 IS ON
AND RED CLEAR ON PHASE #7 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #39 ON
SET OUTPUT ASSIGNMENT #40 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR PHASE 7 RED CLEAR WHEN TRANSITIONING FROM PHASE 7 TO PHASE 8 (HEAD 71).

```

LOGICAL I/O COMMAND #11 (+/-COMMAND#)
IF ACTIVE PHASE #7 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #41 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 7 (HEAD 71).

```

LOGICAL I/O COMMAND #12 (+/-COMMAND#)
IF YELLOW ON PHASE #7 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #40 ON
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 7 (HEAD 71).


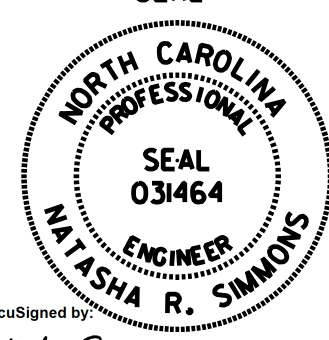
LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OUTPUT REFERENCE SCHEDULE	
USE TO INTERPRET LOGIC PROCESSOR	
OUTPUT 39 =	Overlap D Red
OUTPUT 40 =	Overlap D Yellow
OUTPUT 41 =	Overlap D Green
OUTPUT 42 =	Overlap C Red
OUTPUT 43 =	Overlap C Yellow
OUTPUT 44 =	Overlap C Green
OUTPUT 47 =	Overlap B Red
OUTPUT 48 =	Overlap B Yellow
OUTPUT 49 =	Overlap B Green
OUTPUT 50 =	Overlap A Red
OUTPUT 51 =	Overlap A Yellow
OUTPUT 52 =	Overlap A Green

THIS ELECTRICAL DETAIL IS FOR  
THE SIGNAL DESIGN: 03-0215T1  
DESIGNED: June 2017  
SEALED: 9/10/2021  
REVISED: N/A

Electrical Detail - Sheet 2 of 8  
Signal Upgrade  
Temporary Design 1

**DOCUMENT NOT CONSIDERED FINAL  
UNLESS ALL SIGNATURES COMPLETED**

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	PLAN DATE: June 2017    REVIEWED BY: A.D. Klinksiek PREPARED BY: A.H. Thornburg    REVIEWED BY: N.R. Simmons	REVISIONS    INIT.    DATE _____    _____    _____ _____    _____    _____

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SIG. INVENTORY NO. 03-0215T1