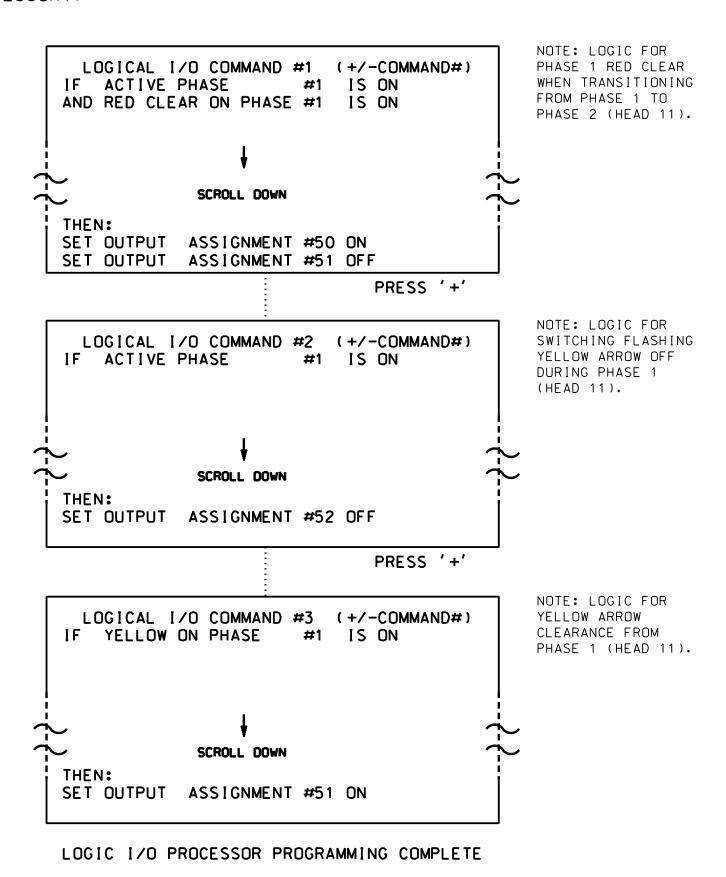
PROJECT REFERENCE NO. U-4906 Sig. 4.2

TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



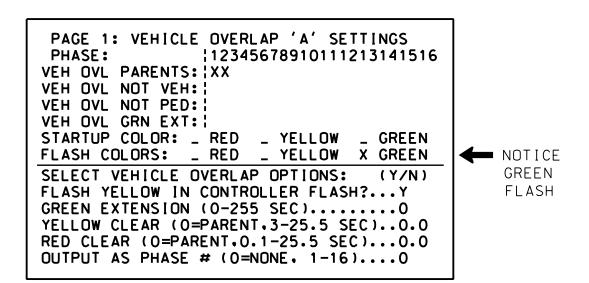
OUTPUT REFERENCE SCHEDULE

USE TO INTERPRET LOGIC PROCESSOR OUTPUT 50 = Overlap A Red OUTPUT 51 = Overlap A Yellow OUTPUT 52 = Overlap A Green

OVERLAP PROGRAMMING DETAIL FOR DEFAULT PHASING

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS). THEN '1' (VEHICLE OVERLAP SETTINGS).



OVERLAP PROGRAMMING COMPLETE

OVERLAP PROGRAMMING DETAIL FOR ALTERNATE PHASING

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS). THEN '1' (VEHICLE OVERLAP SETTINGS). PRESS 'NEXT' TO ADVANCE TO PAGE 2.



PAGE 2: VEHICLE OVERLAP 'A' SETTINGS ¦12345678910111213141516 PHASE: VEH OVL PARENTS: X VEH OVL NOT VEH: | VEH OVL NOT PED: | VEH OVL GRN EXT: : STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW _ GREEN SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?...Y GREEN EXTENSION (0-255 SEC)..... YELLOW CLEAR (O=PARENT.3-25.5 SEC)..0.0 RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

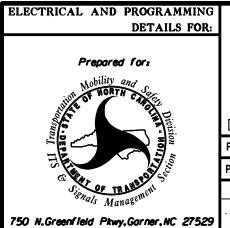
OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 03-0889T1 DESIGNED: October 2018 SEALED: 6/30/2021 REVISED: N/A

Electrical Detail - Sheet 2 of 4 Signal Upgrade

Temporary Design

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



SR 1308 (Gum Branch Road) PLAN DATE: REVISIONS

SR 1324 (Ramsey Road)

TH CARO 031464

SIG. INVENTORY NO. 03-0889T1

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October 2018 REVIEWED BY: A.D. Klinksiek PREPARED BY: A.H. Thornburg REVIEWED BY: N.R. Simmons INIT. DATE