DocuSign Envelope ID: 298FF5ED-1578-4C5D-8EBD-DAA267E00380

PROJECT REFERENCE NO.	SHEET NO.
U-5942	Sig. 28.2

ECONOLITE ASC/3-2070 LOGIC PROCESSOR PROGRAMMING DETAIL FOR PREEMPT ONLY PHASE

(program controller as shown)

The following logic processor configuration omits phase 5 on FYA head (signal 51) for the duration of the normal phase cycle and at startup until preemt activating phase is called to activate phase 5.

1. From Main Menu select 1. CONFIGURATION
2. From CONFIGURATION Submenu select 8. LOGIC PROCESSOR
3. From the LOGIC PROCESSOR Submenu select 2. LOGIC STATEMENTS

ENTER A "1" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:   1  COPY FROM:   1  ACTIVE:  M   (T/F)
IF    PMT PREEMPT ACTIVE    5     IS   OFF

THEN  CTR OMIT PHASE        5         ON

ELSE
```

LOGIC FOR OMMITTING PHASE 5 AT STARTUP AND/OR WHEN NOT IN PREEMPT

4. From the LOGIC PROCESSOR Submenu select 1. LOGIC STATEMENT CONTROL

ENABLE LOGIC PROCESSOR STATEMENTS 1-4 BY POSITIONING THE CURSOR OVER THE FIELDS SHOWN BELOW AND USING THE TOGGLE KEY TO ENABLE THEM .

LOGIC STATEMENT CONTROL

	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6
LP 1-15	E	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
LP 16-30	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
LP 31-45	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
LP 46-60	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
LP 61-75	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
LP 76-90	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.

END PROGRAMMING

ECONOLITE ASC/3-2070 OVERLAP PROGRAMMING DETAIL

(program controller as shown)

1. From Main Menu select 2. CONTROLLER
2. From CONTROLLER Submenu select 2. VEHICLE OVERLAPS

OVERLAP A

Select TMG VEH OVLP [A] and 'PPLT FYA'

```
TMG VEH OVLP...[A] TYPE: .....PPLT FYA

PROTECTED LEFT TURN....   PHASE    1
OPPOSING THROUGH.......   PHASE    2

FLASHING ARROW OUTPUT.....CH9  ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE........... 0
```

Toggle Twice

OVERLAP C

Select TMG VEH OVLP [C] and 'PPLT FYA'

```
TMG VEH OVLP...[C] TYPE: .....PPLT FYA

PROTECTED LEFT TURN....   PHASE    5
OPPOSING THROUGH.......   PHASE    6

FLASHING ARROW OUTPUT.....CH11 ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE........... 0
```

END PROGRAMMING

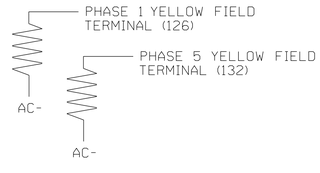
THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 01-0404
DESIGNED: MARCH 2018
SEALED: 08/21/2018
REVISED: N/A

LOAD RESISTOR INSTALLATION DETAIL

(install resistors as shown)

ACCEPTABLE VALUES

VALUE (ohms)	WATTAGE
1.5K - 1.9K	25W (min)
2.0K - 3.0K	10W (min)



Electrical Detail - Sheet 2 of 3

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED

Plans Prepared By:

DRMP, Inc.
8000 Regency Parkway, Suite 175
Cary, NC 27518
NC License No. C-2213 (919) 650-1038

ELECTRICAL AND PROGRAMMING DETAILS FOR:

Prepared for the Offices of:

Traffic Engineering Branch, Mobility and Safety Division, Signals Management Section, NC Department of Transportation

750 N.Greenfield Pkwy,Garner,NC 27529

US 17-158 (N. Road Street) at SR 1387 (Knobbs Creek Road)/ Commercial Drive

Division 1 Pasquotank County Elizabeth City

PLAN DATE:	March 2018	REVIEWED BY:	AJ Davis
PREPARED BY:	DJ White	REVIEWED BY:	LM Moon

REVISIONS	INIT.	DATE

SEAL

NORTH CAROLINA PROFESSIONAL SEAL 022516 ENGINEER LISA M. MOON

DocuSigned by: Lisa M Moon 9/20/2018
5BCE5BDB3D0421

SIG. INVENTORY NO. 01-0404

20-SEP-2018 18:51
R:\U5942Signs\Design\Wiring\01-0404-08212018e.dgn
lmoon AT CAR-LMOON1-W7