Sig. 6.3 U-5942

ECONOLITE ASC/3-2070 LOGIC PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown)

- 1. From Main Menu select | 1. CONFIGURATION |
- 2. From CONFIGURATION Submenu select 8. LOGIC PROCESSOR
- 3. From the LOGIC PROCESSOR Submenu select 2. LOGIC STATEMENTS

ENTER A "1" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#: 1 COPY FROM: 1 ACTIVE: M (T/F) IF PMT PREEMPT ACTIVE 3 IS OFF AND PMT PREEMPT ACTIVE 4 IS OFF THEN CTR OMIT PHASE 1 ELSE

LOGIC FOR OMMITTING PHASE 1 AT START UP AND/OR WHEN NOT IN

4. From the LOGIC PROCESSOR Submenu select 1. LOGIC STATEMENT CONTROL

ENABLE LOGIC PROCESSOR STATEMENT 1 BY POSITIONING THE CURSOR OVER THE FIELDS SHOWN BELOW AND USING THE TOGGLE KEY TO ENABLE THEM .

LOGIC STATEMENT CONTROL

END PROGRAMMING

ECONOLITE ASC/3-2070 OVERLAP

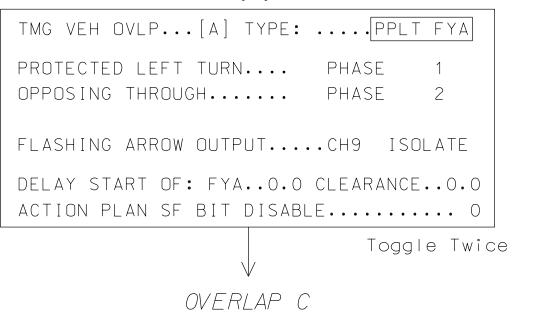
PROGRAMMING DETAIL

(program controller as shown)

- 1. From Main Menu select | 2. CONTROLLER
- 2. From CONTROLLER Submenu select 2. VEHICLE OVERLAPS

OVERLAP A

Select TMG VEH OVLP [A] and 'PPLT FYA'



Select TMG VEH OVLP [C] and 'OTHER/ECONOLITE'

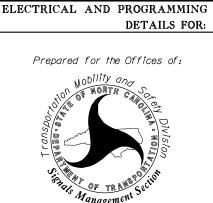
		L -]						
TMG VEH OVLP	TYPE: OTHER/ECONOLITE								
PHASES 1 2 3	4 5	6	78	9 () 1	2 3	3 4	5	6
INCLUDED		X .		•		0 0	•	•	•
PROTECT	e e	Θ (•	e e	e e	•	6	
PED PRTC		•		•			•	•	•
NOT OVLP		•		•		• •	•	•	•
FLSH GRN		1 .				e e	6		
LAG X PH	9 9		9 9			e e	8		
LAG 2 PH · · ·		•	• •	•	• •		•	•	•
LAG GRN 0.0 YEL	_ ().() RE	ED (0.0	AD\	/ GF	5N ().()

END PROGRAMMING

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 01-0008 DESIGNED: FEBRUARY 2018 SEALED: 09/20/2018 REVISED: N/A

Electrical Detail - Sheet 3 of 5

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



US 158 (Elizabeth Street)

N. MLK Junior Drive

Division 1 Pasquotank County Elizabeth City PLAN DATE: February 2018 REVIEWED BY: AJ Davis PREPARED BY: DJ White REVIEWED BY: LM Moon REVISIONS INIT. DATE

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Lisa M. Moon 9/20/2018