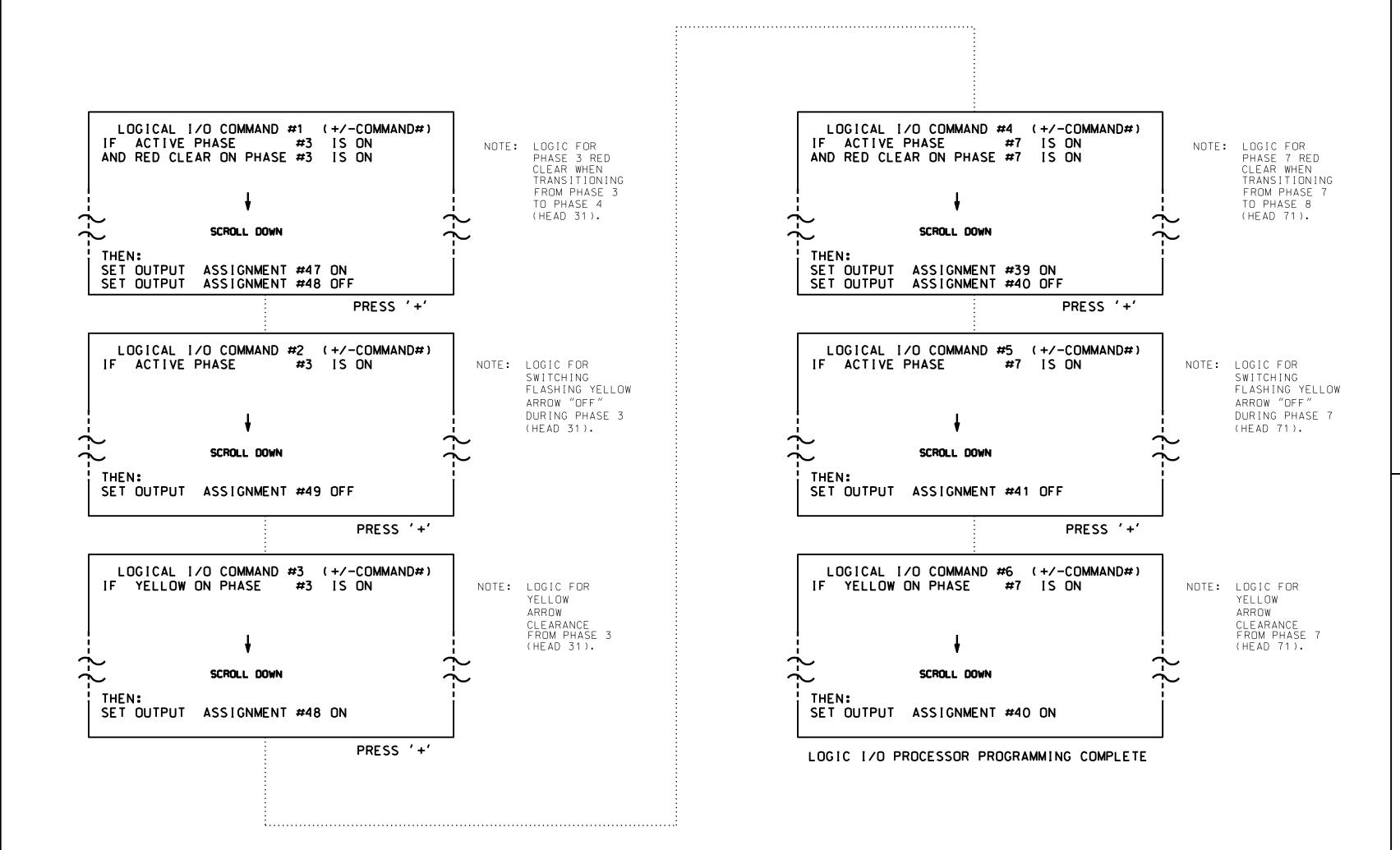
## LOGICAL I/O PROCESSOR PROGRAMMING DETAIL

## TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, AND 6.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS). THEN '3' (LOGICAL I/O PROCESSOR).



OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS). THEN '1' (VEHICLE OVERLAP SETTINGS).

PAGE 1: VEHICLE OVERLAP 'B' SETTINGS 12345678910111213141516 VEH OVL NOT VEH: VEH OVL NOT PED: VEH OVL GRN EXT: : STARTUP COLOR: \_ RED \_ YELLOW \_ GREEN FLASH COLORS: \_ RED \_ YELLOW X GREEN NOTICE GREEN FLASH SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?...N GREEN EXTENSION (0-255 SEC)..... YELLOW CLEAR (O=PARENT.3-25.5 SEC)..0.0 RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

PAGE 1: VEHICLE OVERLAP 'D' SETTINGS 12345678910111213141516 PHASE: VEH OVL PARENTS:: XX VEH OVL NOT VEH: VEH OVL NOT PED: : VEH OVL GRN EXT: | STARTUP COLOR: \_ RED \_ YELLOW \_ GREEN FLASH COLORS: \_ RED \_ YELLOW X GREEN NOTICE GREEN FLASH SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?...N GREEN EXTENSION (0-255 SEC)..... YELLOW CLEAR (O=PARENT.3-25.5 SEC)..0.0 RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

PRESS '+' TWICE

OVERLAP PROGRAMMING COMPLETE

## FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH. MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

- 1. ON REAR OF PDA REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
- 2. ON REAR OF PDA REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
- 3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 04-0111T2 DESIGNED: June 2019 **SEALED:** 3/17/2020 REVISED: N/A

**OUTPUT REFERENCE SCHEDULE** 

USE TO INTERPRET LOGIC PROCESSOR

OUTPUT 39 = Overlap D Red OUTPUT 40 = Overlap D Yellow OUTPUT 41 = Overlap D Green

OUTPUT 48 = Overlap B Yellow OUTPUT 49 = Overlap B Green

OUTPUT 47 = Overlap B Red

NC Firm License No.: F-0342 701 Corporate Center Drive

ELECTRICAL AND PROGRAMMIN DETAILS FOR: Prepared for the Offices of:

I-95 Ramps and NC 4

NC 4 / NC 48

ivision 4 Rocky Moun June 2019 REVIEWED BY: J. O. Deaton PLAN DATE: PREPARED BY: A. Ravipati REVIEWED BY: M. W. Yalch

07438

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED

James O. Deaton

Suite 475 Raleigh, NC 27607 Phone: 919-854-6200

REVISIONS 750 N.Greenfield Pkwy.Garner.NC 27529

Temporary Design 2 (TMP Phase II) Electrical Detail Sheet 2 of 2

SIG. INVENTORY NO. 04-0111T2