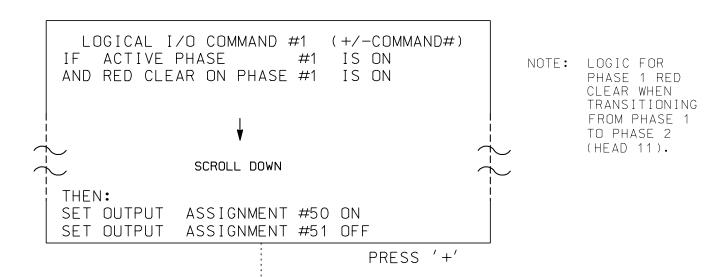
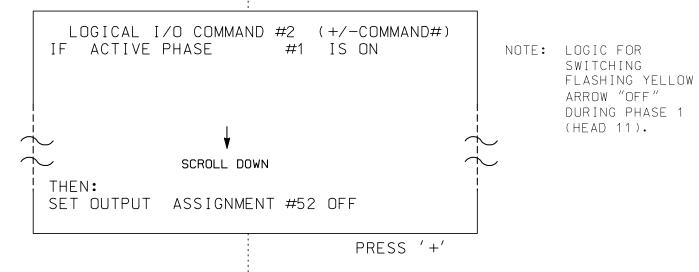
## PROJECT REFERENCE NO. SHEET NO. Sig. 2.2

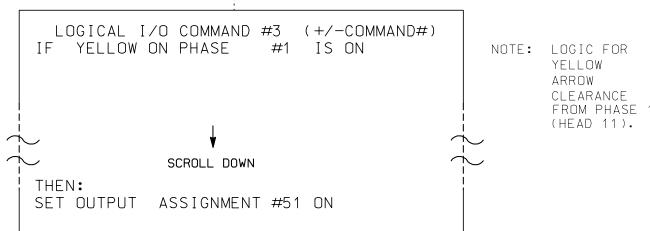
## LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).





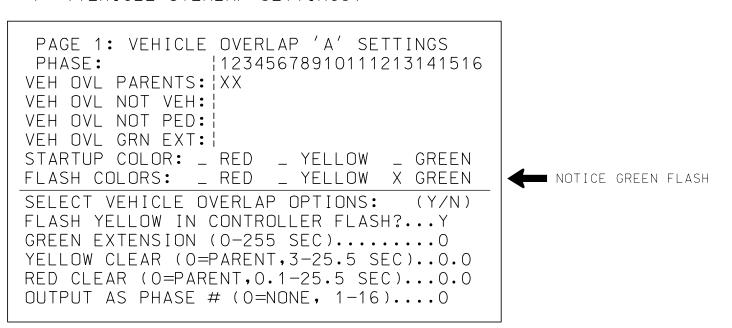


LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

## OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).



OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 14-1021T DESIGNED: JUNE 2019 SEALED: 11-19-2019 REVISED: N/A

Electrical Detail - Temporary Design - Sheet 2 of 2

Mobility and Morth Canonia Single Management

NC 225 (Greenville Highway) at SR 1783 (N. Highland Lake Road)

ivision 14	Henderson County		East Fi	lat Rock
LAN DATE:	June 2019	REVIEWED BY:	R. Dubn	icka
REPARED BY:	J. Trueblood	REVIEWED BY:	J. Carr	011
REVISIONS			INIT.	DATE

SIG. INVENTORY NO. 14-1021T

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED

STV Engineers, Inc.
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Charlotte, NC 28202
(704) 372-1885
NC License Number F-0991

OUTPUT SO = Overlap A Red
OUTPUT 51 = Overlap A Yellow
OUTPUT 52 = Overlap A Green