PROJECT REFERENCE NO.	SHEET NO.
U-2581BA	Sig.2.2

ECONOLITE ASC/3-2070 OVERLAP PROGRAMMING DETAIL

(program controller as shown)

1. From Main Menu select [2. CONTROLLER]
2. From CONTROLLER Submenu select [2. VEHICLE OVERLAPS]

OVERLAP A

Select TMG VEH OVLP [A] and 'PPLT FYA'

```
TMG VEH OVLP...[A] TYPE: .....[PPLT FYA]

PROTECTED LEFT TURN....   PHASE    1
OPPOSING THROUGH.......   PHASE    2

FLASHING ARROW OUTPUT.....CH9  ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE........... 0
```

Toggle Once

OVERLAP B

Select TMG VEH OVLP [B] and 'PPLT FYA'

```
TMG VEH OVLP...[B] TYPE: .....[PPLT FYA]

PROTECTED LEFT TURN....   PHASE    3
OPPOSING THROUGH.......   PHASE    4

FLASHING ARROW OUTPUT.....CH10 ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE........... 0
```

Toggle Once

OVERLAP C

Select TMG VEH OVLP [C] and 'PPLT FYA'

```
TMG VEH OVLP...[C] TYPE: .....[PPLT FYA]

PROTECTED LEFT TURN....   PHASE    5
OPPOSING THROUGH.......   PHASE    6

FLASHING ARROW OUTPUT.....CH11 ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE........... 0
```

END PROGRAMMING

FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

1. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
2. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

ECONOLITE ASC/3-2070 BACKUP PROTECTION ENABLE PROGRAMMING

(program controller as shown)

1. From Main Menu select [1. CONFIGURATION]
2. From CONFIGURATION Submenu select [1. CONTROLLER SEQ]
3. From CONTROLLER SEQUENCE Submenu select [3. BACKUP PREVENT PHASES]

Follow programming as shown below. On the 'ENABLE BACKUP PREVENT' screen move cursor to the appropriate field and press 'YES/NO' on the controller keypad to toggle field value between 'X' ,'B', 'C' and 'OFF'.

ENABLE BACKUP PREVENT

TMG/BKUP	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6
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END PROGRAMMING

NOTES

1. 'X' inhibits the controller from servicing the 'BACKUP' (column) phase when the 'TIMING' (row) phase is active or next.

THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 07-0204T1
DESIGNED: September 2019
SEALED: 09/09/2019
REVISED: N/A

VHB Engineering NC, P.C. (C-3705)
940 Main Campus Drive, Suite 500
Raleigh, NC 27606
P: 919-829-0328

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED

Electrical Detail-Temporary Design 1 (TMP Phase I)-Sheet 2 of 2

ELECTRICAL AND PROGRAMMING DETAILS FOR:

US 70 (Burlington Road)
at
SR 3045/2819
(Mt. Hope Church Road)

Division 7 | Guilford County | Greensboro

PLAN DATE: September 2019	REVIEWED BY: M.L. Stygles
PREPARED BY: J. Ma	REVIEWED BY:

REVISIONS	INIT.	DATE

Prepared for the Offices of: Transportation Mobility and Safety Division, ITS & Signals Management Section, State of North Carolina Department of Transportation
750 N.Greenfield Pkwy,Garner,NC 27529

SEAL
NORTH CAROLINA PROFESSIONAL SEAL 033108 ENGINEER JIANXIN MA

DocuSigned by: Jianxin Ma
827E1953081444F...
9/9/2019
DATE

SIG. INVENTORY NO. 07-0204T1