

LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).

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LOGICAL I/O COMMAND #1 (+/-COMMAND#)
IF ACTIVE PHASE #5 IS ON
AND RED CLEAR ON PHASE #5 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #42 ON
SET OUTPUT ASSIGNMENT #43 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR PHASE 5 RED CLEAR WHEN TRANSITIONING FROM PHASE 5 TO PHASE 6 (HEAD 51).

```

LOGICAL I/O COMMAND #2 (+/-COMMAND#)
IF ACTIVE PHASE #5 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #44 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 5 (HEAD 51).

```

LOGICAL I/O COMMAND #3 (+/-COMMAND#)
IF YELLOW ON PHASE #5 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #43 ON
    
```

NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 5 (HEAD 51).

LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OUTPUT REFERENCE SCHEDULE	
OUTPUT 42 =	Overlap C Red
OUTPUT 43 =	Overlap C Yellow
OUTPUT 44 =	Overlap C Green

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

PRESS '+' TWICE

```

PAGE 1: VEHICLE OVERLAP 'C' SETTINGS
PHASE:      12345678910111213141516
VEH OVL PARENTS:  XX
VEH OVL NOT VEH:
VEH OVL NOT PED:
VEH OVL GRN EXT:
STARTUP COLOR:  _ RED  _ YELLOW  _ GREEN
FLASH COLORS:  _ RED  _ YELLOW  X GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0-255 SEC)...0.0
YELLOW CLEAR (0=PARENT,3-25.5 SEC)...0.0
RED CLEAR (0=PARENT,0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0
    
```

← NOTICE GREEN FLASH

OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 13-0611T2
DESIGNED: FEBRUARY 2019
SEALED: 02/05/2019
REVISED: N/A

Temporary Design 2 - TMP Phase II
Electrical Detail - Sheet 2 of 2

DOCUMENT NOT CONSIDERED FINAL
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	PLAN DATE: January 2019 REVIEWED BY: E D Harris PREPARED BY: G B Spell REVIEWED BY: R M Muncey	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 50%;">REVISIONS</th> <th style="width: 20%;">INIT.</th> <th style="width: 30%;">DATE</th> </tr> <tr> <td> </td> <td> </td> <td> </td> </tr> </table>	REVISIONS	INIT.	DATE			
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