PROJECT REFERENCE NO. U-4405 SIG-38.

ECONOLITE ASC/3-2070 LOGIC PROCESSOR PROGRAMMING DETAIL

(program controller as shown)

- 1. From Main Menu select | 1. CONFIGURATION
- 2. From CONFIGURATION Submenu select | 8. LOGIC PROCESSOR

3. From LOGIC PROCESSOR Submenu select 2. LOGIC STATEMENTS

ENTER A "1" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#:	1	COPY	FROM:	1	ACTIVE:	М	FALSE	
ΙF	CTR	PHASE	TMING		1	ΙS	ON	
THEN	SIG	SET O	LP GREE	N	1		OFF	
ELSE								

LOGIC FOR TURNING FLASHING YELLOW ARROW OFF DURING PHASE 1 (HEADS 83,84)

ENTER A "2" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#:	2	COPY FROM:	2	ACTIVE:	М	FALSE	
ΙF	VEH	YELLOW ON	PH	1	IS	ON	
THEN	SIG	SET OLP YE	LLOW	1		ON	
ELSE							

LOGIC FOR YELLOW ARROW CLEARANCE WHEN LEAVING PHASE 1 (HEADS 83,84)

ENTER A "3" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#:	3	COPY	FROM:	3	ACTIVE:	М	FALSE
			E TIMING ON PHASE		1 1	IS IS	O .,
THEN	SIG	SET	OLP RED		1		ON
ELSE							

LOGIC FOR RED SIGNAL CLEARANCE WHEN LEAVING PHASE 1 (HEADS 83,84)

ENTER A "4" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#:	4 COPY FROM: 4	ACTIVE:	M FALSE	
ΙF	CTR PHASE TMING	5	IS ON	
THEN	SIG SET OLP GREEN	3	OFF	
ELSE				

FLASHING YELLOW ARROW OFF DURING PHASE 5 (HEADS 43,44)

LOGIC FOR TURNING

ENTER A "5" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#:	5	COPY FROM:	5	ACTIVE:	М	FALSE
ΙF	VEH	YELLOW ON PH	Н	5	IS	ON
THEN	SIG	SET OLP YELL	_OW	3		ON
ELSE						

LOGIC FOR YELLOW ARROW CLEARANCE WHEN LEAVING PHASE 5 (HEADS 43,44)

ENTER A "6" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#:	6	COPY	FROM:	6	ACTIVE:	М	FALSE
_	_		E TIMING ON PHASE		5 5	IS IS	ON ON
THEN	SIG	SET	OLP RED		3		ON
ELSE							

LOGIC FOR RED SIGNAL CLEARANCE WHEN LEAVING PHASE 5 (HEADS 43,44)

ENTER A "7" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#:	7	COPY FROM	M: 7	ACTIVE:	М	FALSE
ΙF	VEH	OVERLAP		8	IS	ON
THEN	SIG	SET OVLP	GREEN	4		OFF
ELSE						

LOGIC FOR TURNING FLASHING YELLOW ARROW OFF DURING OLH, WHICH HAS PARENT PHASE 3 (HEADS 23,24)

ENTER A "8" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#:	8	COPY FROM:	8	ACTIVE:	М	FALSE
ΙF	VEH	OVERLAP YLW		8	ΙS	ON
THEN	SIG	SET OLP YELLO	W	4		ON
ELSE						

LOGIC FOR YELLOW ARROW CLEARANCE WHEN LEAVING OLH, WHICH HAS PARENT PHASE 3 (HEADS 23,24)

LOGIC FOR RED SIGNAL

LEAVING OLH, WHICH

HAS PARENT PHASE 3

CLEARANCE WHEN

(HEADS 23,24)

ENTER A "9" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#:	9	COPY FRO	CM:	9	ACTIVE:	М	FALSE	
		OVERLAP OVERLAP	RED		8 8	IS IS		
THEN	SIG	SET OLP	RED		4		ON	
ELSE								

END PROGRAMMING

4. From LOGIC PROCESSOR Submenu select | 1. LOGIC STATEMENT CONTROL

ENABLE LOGIC PROCESSOR STATEMENTS 1-9 BY POSITIONING THE CURSOR OVER THE FIELDS SHOWN BELOW AND USING THE TOGGLE KEY TO ENABLE THEM.

_																		
LOGIC STATEMENT			CO	CONTROL														
			1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	
	LΡ	1-15	Ε	Ε	Ε	Ε	Ε	Ε	Ε	Ε	Ε	•	•	•	•	•	•	
	LΡ	16-30	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	
	LΡ	31-45	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	
	LΡ	46-60	•		•	•	•	•	•	•	•	•	•	•	•	•	•	
	LΡ	61-75	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	
	LΡ	76-90	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	

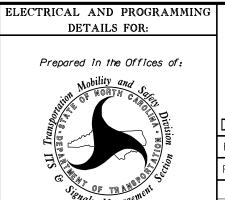
END PROGRAMMING

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 06-0155T3 DESIGNED: March 2018 SEALED: 03-29-2018 REVISED: N/A

Temporary Design 3 - TMP Phase III Electrical Detail - Sheet 3 of 3



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Division 6 Cumberland County Fayetteville March 2018 REVIEWED BY: PLAN DATE: L Overn PREPARED BY: G B Spell REVIEWED BY: REVISIONS INIT. DATE

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