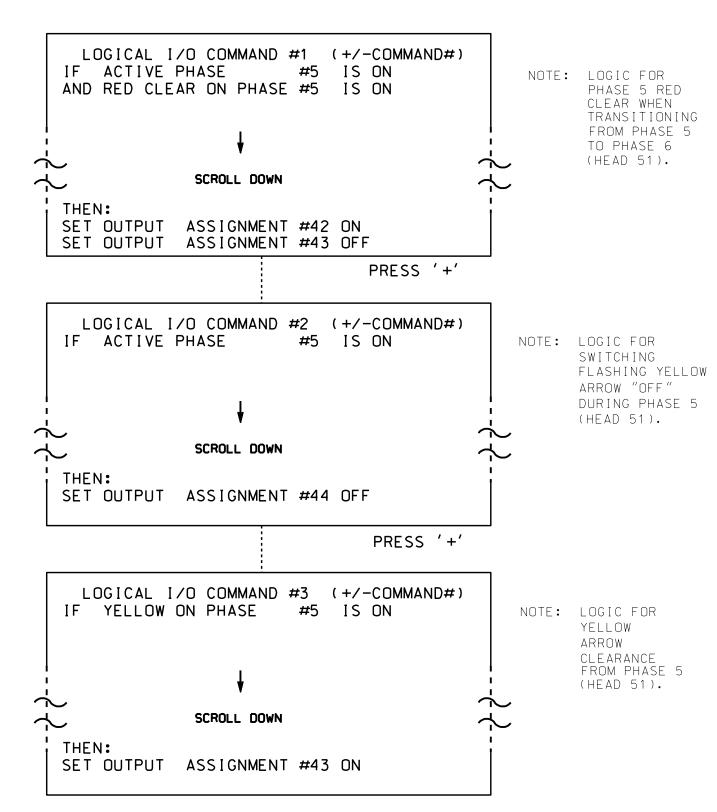
(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2 AND 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OUTPUT REFERENCE SCHEDULE

OUTPUT 42 = Overlap C Red
OUTPUT 43 = Overlap C Yellow
OUTPUT 44 = Overlap C Green

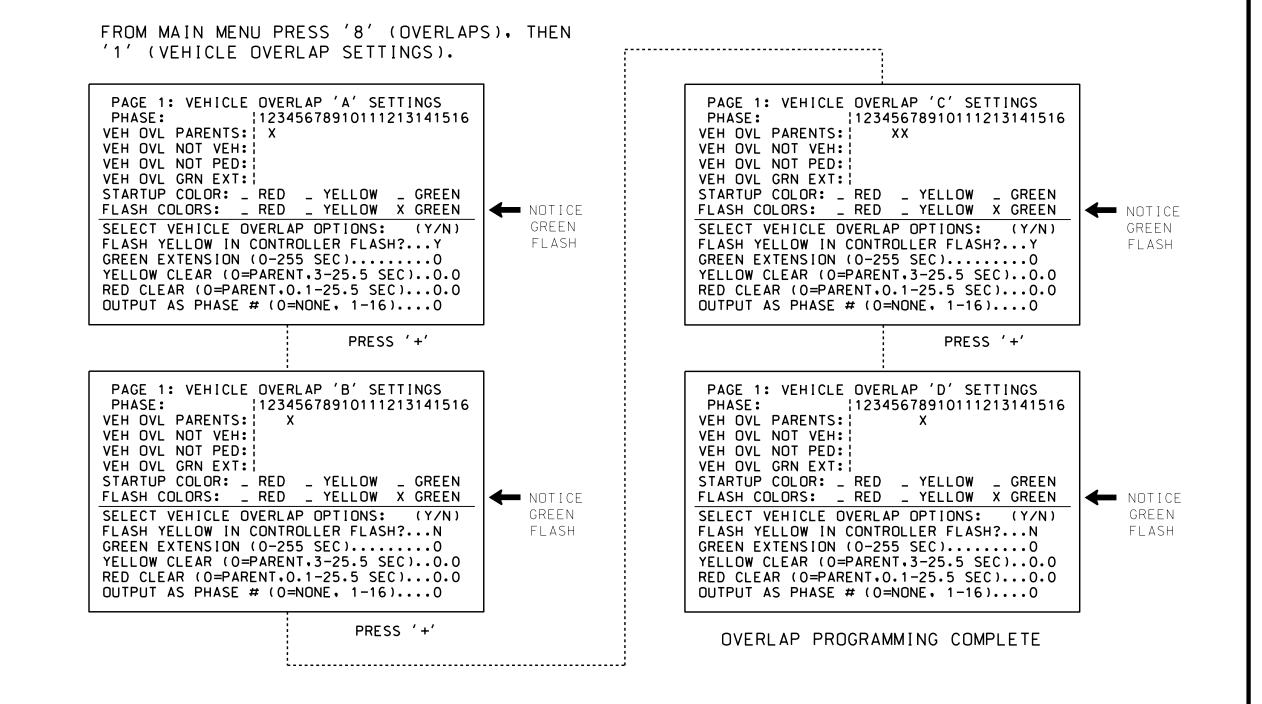
U - 5963

PROJECT REFERENCE NO.

Sig. 5.2

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)



FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

- 1. ON REAR OF PDA REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
- 2. ON REAR OF PDA REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
- 3. REMOVE FLASHER UNIT 2.

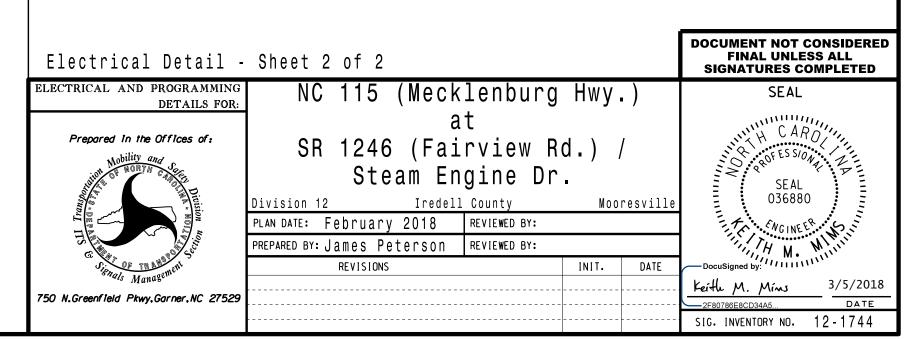
THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 12-1744

DESIGNED: January 2018

SEALED: 02-27-18

REVISED: N/A



5.*TISASUATIS SIGNOLS*MON NG OUPSASIG MANAFERENSON *121744_SMLENE. jtpeterson