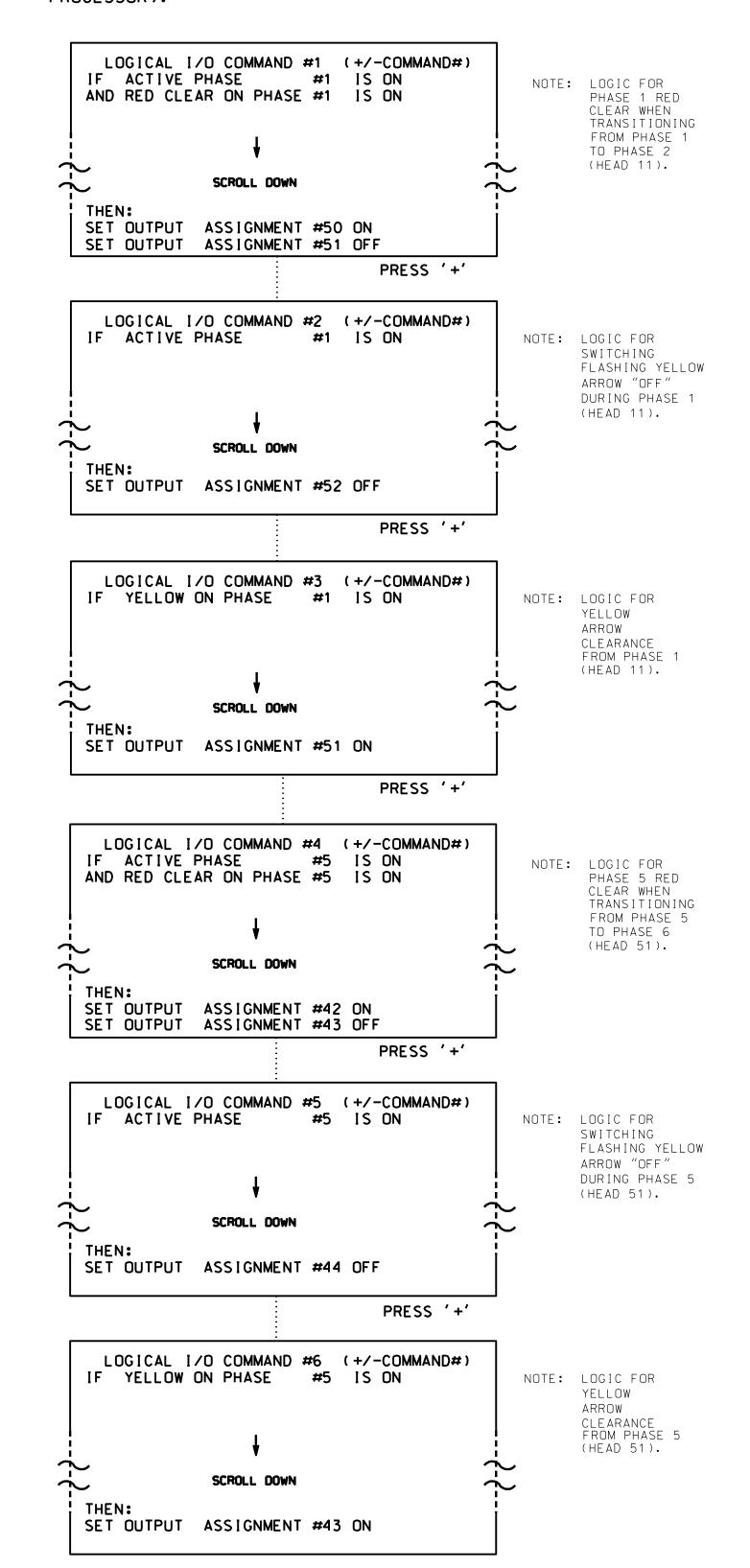
## LOGICAL I/O PROCESSOR PROGRAMMING DETAIL

## TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL). THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1. 2. 3. 4. 5. AND 6.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

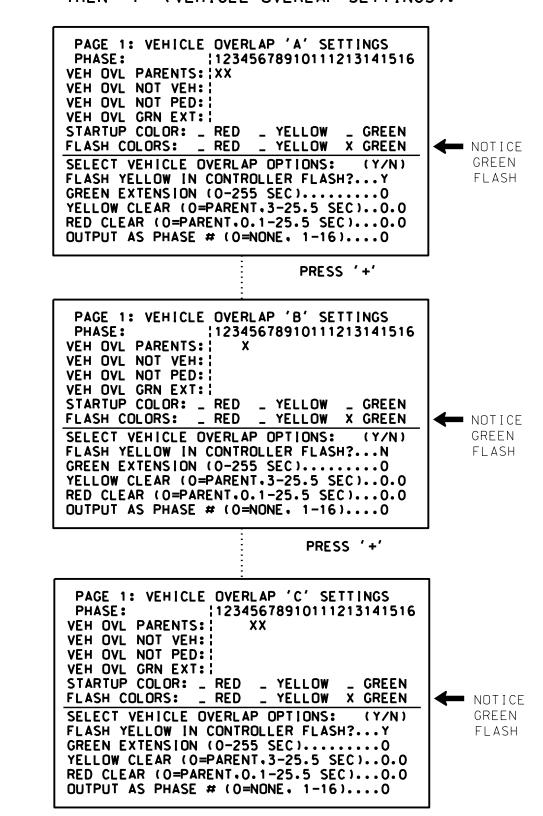
## OUTPUT REFERENCE SCHEDULE USE TO INTERPRET LOGIC PROCESSOR OUTPUT 42 = Overlap C Red OUTPUT 43 = Overlap C Yellow OUTPUT 44 = Overlap C Green OUTPUT 50 = Overlap A Red OUTPUT 51 = Overlap A Yellow OUTPUT 52 = Overlap A Green

U-5169 Sig. 18.2

## OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS).
THEN '1' (VEHICLE OVERLAP SETTINGS).



OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 07-1470T2
DESIGNED: May 2018
SEALED: May 20, 2018
REVISED: N/A

Project #: 170908

**DOCUMENT NOT CONSIDERED** 

FINAL UNLESS ALL



Temporary Design 2; TMP-25
Electrical Detail - Sheet 2 of 3

Prepared for:

Outsion 7 Guilford County High Prepared By: A. Ravipati Reviewed By:

Revisions Init.

SEAL

Point

DocuSigned by:

SEAL

OS /20 /201

PREPARED BY: A. Ravipati REVIEWED BY:

REVISIONS

INIT. DATE

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