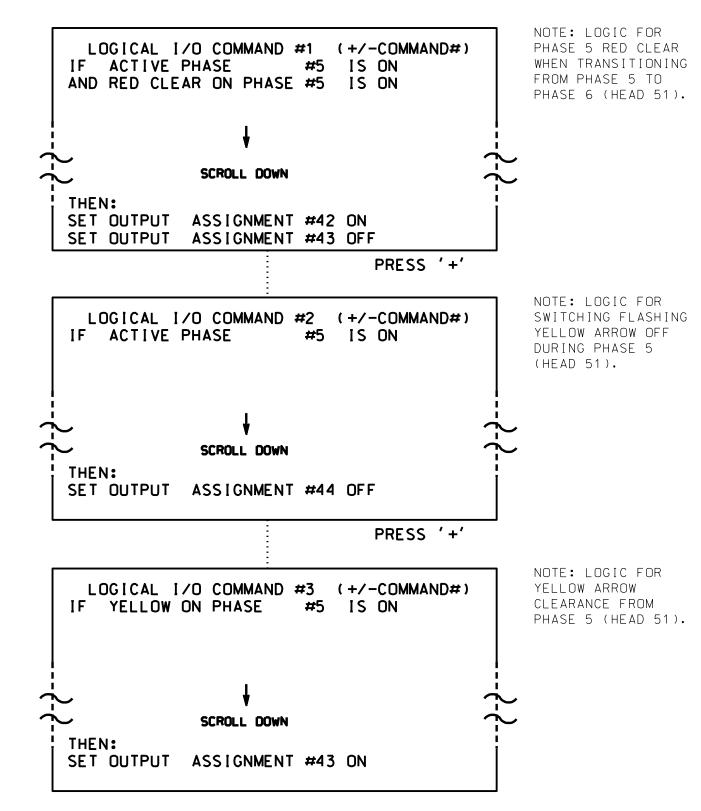
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS). THEN '3' (LOGICAL I/O PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

REFERENCE SCHEDULE USE TO INTERPRET LOGIC PROCESSOR

OUTPUT 42 = Overlap C Red OUTPUT 43 = Overlap C Yellow

OUTPUT 44 = Overlap C Green

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS). THEN '1' (VEHICLE OVERLAP SETTINGS).

PRESS '+' TWICE

PAGE_1: VEHICLE OVERLAP 'C' SETTINGS 12345678910111213141516 VEH OVL PARENTS: | XX VEH OVL NOT VEH: VEH OVL NOT PED: VEH OVL GRN EXT: |
STARTUP COLOR: _ RED _ YELLOW _ GREEN
FLASH COLORS: _ RED _ YELLOW X GREEN

NOTICE SELECT VEHICLE OVERLAP OPTIONS: (Y/N) GREEN FLASH YELLOW IN CONTROLLER FLASH?...Y FLASH GREEN EXTENSION (0-255 SEC).....0 YELLOW CLEAR (0=PARENT.3-25.5 SEC)..0.0 RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 07-1623T1 DESIGNED: May 2018 SEALED: May 18, 2018 REVISED: N/A

PROJECT REFERENCE NO.

U-5169

¹Sig. 10.2

Project #: 170908



Temporary Design 1; TMP-6 Electrical Detail Sheet 2 of 2

ELECTRICAL AND PROGRAMMIN

NC 68 (Eastchester Drive)

I-74 WB/ US 311 NB Ramps

Guilford County PLAN DATE: May 2018 REVIEWED BY: L. Bover PREPARED BY: A Ravipati REVIEWED BY: R. Hinshaw REVISIONS INIT. DATE

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL
SIGNATURES COMPLETED

SIG. INVENTORY NO. 07-1623T1