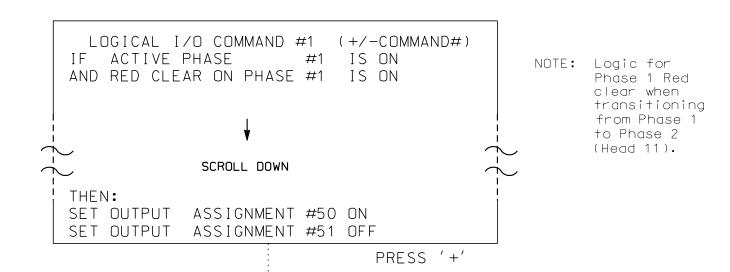
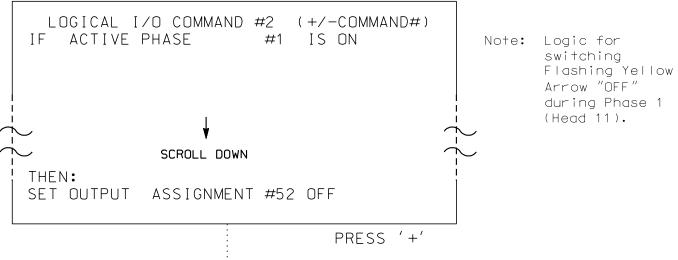
PROJECT REFERENCE NO. Sig. 4.2 U-2412A

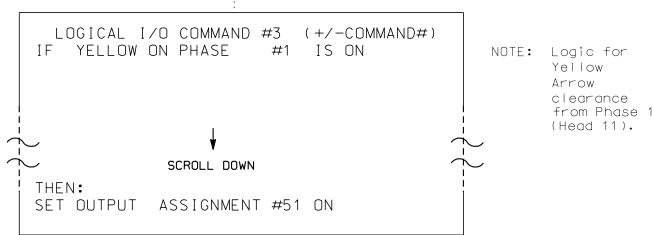
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. From Main Menu press '2' (PHASE CONTROL), then '1' (PHASE CONTROL FUNCTIONS). Scroll to the bottom of the menu and Enable ACT Logic Commands 1, 2 and 3.
- 2. From Main Menu press '6' (OUTPUTS), then '3' (LOGICAL I/O PROCESSOR).







OUTPUT REFERENCE SCHEDULE

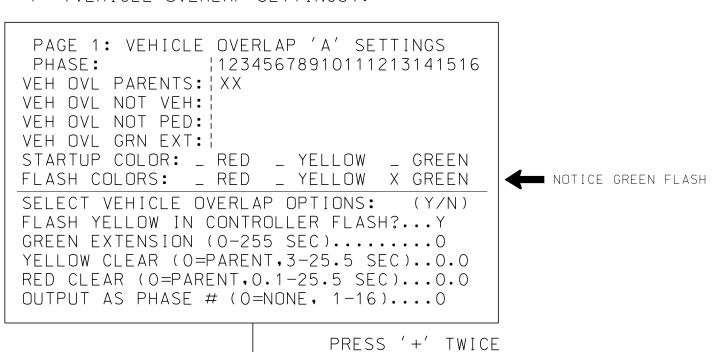
LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OUTPUT 50 = Overlap A Red OUTPUT 51 = Overlap A Yellow OUTPUT 52 = Overlap A Green

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

From Main Menu press '8' (OVERLAPS), then '1' (VEHICLE OVERLAP SETTINGS).

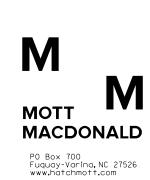


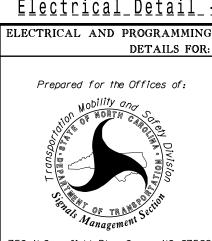
PAGE 1: VEHICLE OVERLAP 'C' SETTINGS PHASE: 12345678910111213141516 VEH OVL PARENTS: | VEH OVL NOT VEH: | VEH OVL NOT PED: | VEH OVL GRN EXT: | STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW X GREEN NOTICE GREEN FLASH SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?...Y GREEN EXTENSION (0-255 SEC)..... YELLOW CLEAR (O=PARENT,3-25.5 SEC)..0.0 RED CLEAR (0=PARENT, 0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: ØZ-1272__ DESIGNED: February 2018 SEALED: REVISED: N/A_____

Temporary Design <u>Electrical_Detail_-_Sheet_2_of_2____</u>





SR 1486 (Greensboro Road) Enterprise Dr./Spencer Street

Division 7 Guilford County High Point PLAN DATE: February 2018 REVIEWED BY: R. Thompson PREPARED BY: B. Lehan REVIEWED BY: T. Pate REVISIONS INIT. DATE

SIG. INVENTORY NO. 07-1272T