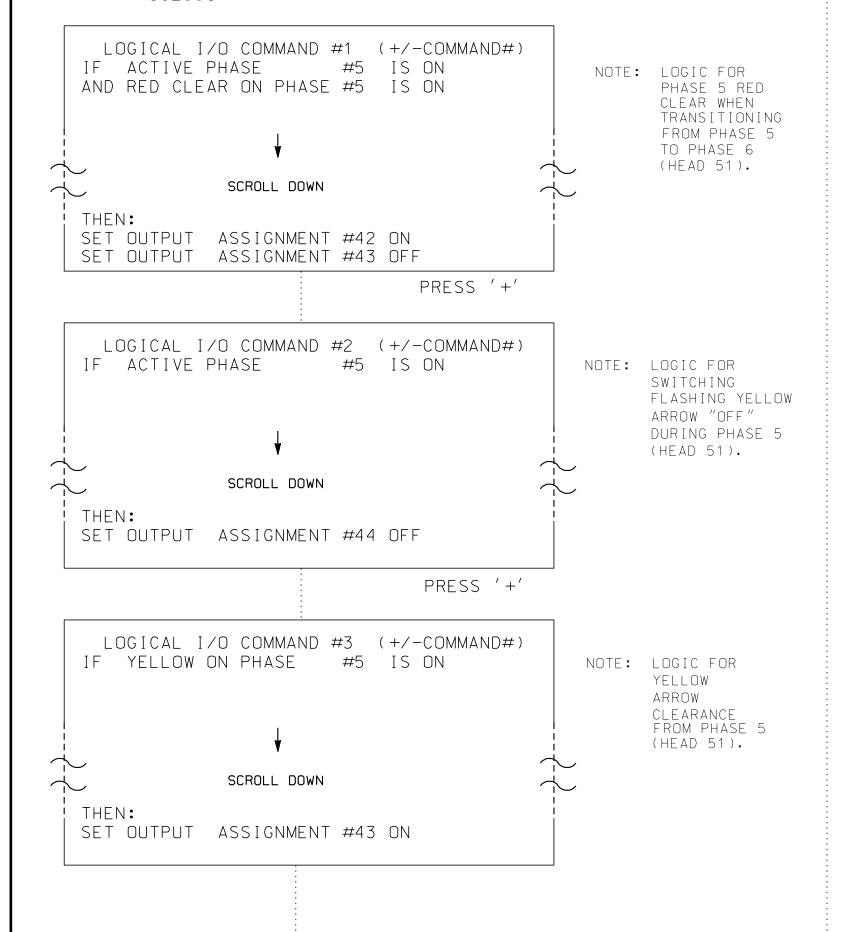
PROJECT REFERENCE NO. SHEET NO. U-2412A Sig. 2.2

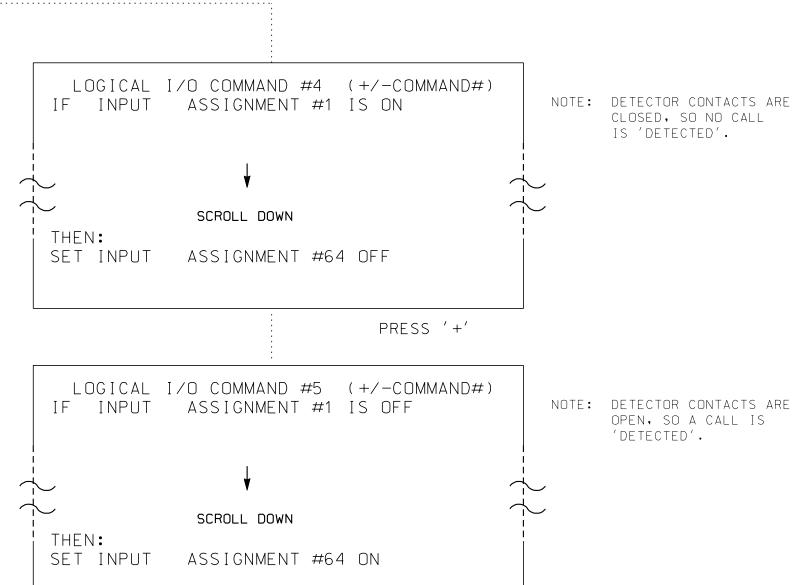
# LOGICAL I/O PROCESSOR PROGRAMMING DETAIL

## TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS), SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, AND 5.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).





LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

#### OUTPUT REFERENCE SCHEDULE

INPUT 1 = Detector Physical Input (Not Enabled)
INPUT 64 = Dummy Detector Input (Detector 2)

OUTPUT 42 = Overlap C Red
OUTPUT 43 = Overlap C Yellow

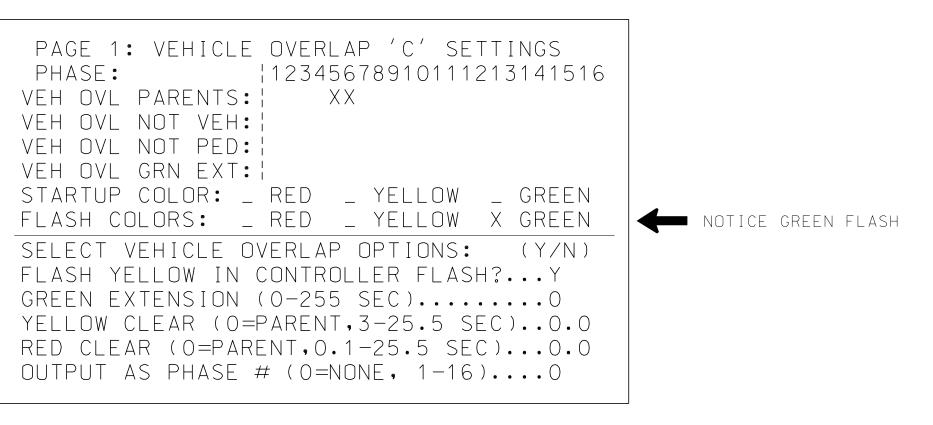
OUTPUT 44 = Overlap C Green

### OVERLAP PROGRAMMING DETAIL

#### (program controller as shown below)

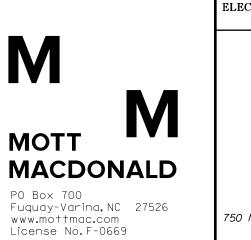
FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

PRESS '+' TWICE



OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: Ø7-1592
DESIGNED: February 2018
SEALED: 3/20/2018
REVISED: \_\_\_\_\_



Electrical Detail - Sheet 2 of 3

ELECTRICAL AND PROGRAMMING DETAILS FOR:

SR 1486

Prepared for the Offices of:

I - 74 WE
Division 7 Gu
PLAN DATE: Februar
PREPARED BY: B. L
REVISIONS

750 N.Greenfield Pkwy,Garner,NC 27529

Temporary Design

SR 1486 (Greensboro Road) at I-74 WB/US 311 NB Ramps

Division 7 Guilford County High Point
PLAN DATE: February 2018 REVIEWED BY: T. Pate
PREPARED BY: B. Lehan REVIEWED BY: R. Thompson
REVISIONS INIT. DATE

**DOCUMENT NOT CONSIDERED**