

LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS), SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, AND 12.
2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).

```

LOGICAL I/O COMMAND #1 (+/-COMMAND#)
IF ACTIVE PHASE #1 IS ON
AND RED CLEAR ON PHASE #1 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #50 ON
SET OUTPUT ASSIGNMENT #51 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR PHASE 1 RED CLEAR WHEN TRANSITIONING FROM PHASE 1 TO PHASE 2 (HEAD 11).

```

LOGICAL I/O COMMAND #2 (+/-COMMAND#)
IF ACTIVE PHASE #1 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #52 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 1 (HEAD 11).

```

LOGICAL I/O COMMAND #3 (+/-COMMAND#)
IF YELLOW ON PHASE #1 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #51 ON
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 1 (HEAD 11).

```

LOGICAL I/O COMMAND #4 (+/-COMMAND#)
IF ACTIVE PHASE #5 IS ON
AND RED CLEAR ON PHASE #5 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #42 ON
SET OUTPUT ASSIGNMENT #43 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR PHASE 5 RED CLEAR WHEN TRANSITIONING FROM PHASE 5 TO PHASE 6 (HEAD 51).

```

LOGICAL I/O COMMAND #5 (+/-COMMAND#)
IF ACTIVE PHASE #5 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #44 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 5 (HEAD 51).

```

LOGICAL I/O COMMAND #6 (+/-COMMAND#)
IF YELLOW ON PHASE #5 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #43 ON
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 5 (HEAD 51).

```

LOGICAL I/O COMMAND #7 (+/-COMMAND#)
IF ACTIVE PHASE #3 IS ON
AND RED CLEAR ON PHASE #3 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #47 ON
SET OUTPUT ASSIGNMENT #48 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR PHASE 3 RED CLEAR WHEN TRANSITIONING FROM PHASE 3 TO PHASE 4 (HEAD 31).

```

LOGICAL I/O COMMAND #8 (+/-COMMAND#)
IF ACTIVE PHASE #3 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #49 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 3 (HEAD 31).

```

LOGICAL I/O COMMAND #9 (+/-COMMAND#)
IF YELLOW ON PHASE #3 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #48 ON
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 3 (HEAD 31).

```

LOGICAL I/O COMMAND #10 (+/-COMMAND#)
IF ACTIVE PHASE #7 IS ON
AND RED CLEAR ON PHASE #7 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #39 ON
SET OUTPUT ASSIGNMENT #40 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR PHASE 7 RED CLEAR WHEN TRANSITIONING FROM PHASE 7 TO PHASE 8 (HEAD 71).

```

LOGICAL I/O COMMAND #11 (+/-COMMAND#)
IF ACTIVE PHASE #7 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #41 OFF
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 7 (HEAD 71).

```

LOGICAL I/O COMMAND #12 (+/-COMMAND#)
IF YELLOW ON PHASE #7 IS ON
    ↓
    SCROLL DOWN
    ↓
THEN:
SET OUTPUT ASSIGNMENT #40 ON
    ↓
    PRESS '+'
    
```

NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 7 (HEAD 71).

LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

```

PAGE 1: VEHICLE OVERLAP 'A' SETTINGS
PHASE: 12345678910111213141516
VEH OVL PARENTS: XX
VEH OVL NOT VEH:
VEH OVL NOT PED:
VEH OVL GRN EXT:
STARTUP COLOR: - RED - YELLOW - GREEN
FLASH COLORS: - RED - YELLOW X GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0=255 SEC)...0
YELLOW CLEAR (0=PARENT.3-25.5 SEC)...0.0
RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0
    ↓
    PRESS '+'
    
```

← NOTICE GREEN FLASH

```

PAGE 1: VEHICLE OVERLAP 'B' SETTINGS
PHASE: 12345678910111213141516
VEH OVL PARENTS: XX
VEH OVL NOT VEH:
VEH OVL NOT PED:
VEH OVL GRN EXT:
STARTUP COLOR: - RED - YELLOW - GREEN
FLASH COLORS: - RED - YELLOW X GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...N
GREEN EXTENSION (0=255 SEC)...0
YELLOW CLEAR (0=PARENT.3-25.5 SEC)...0.0
RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0
    ↓
    PRESS '+'
    
```

← NOTICE GREEN FLASH

```

PAGE 1: VEHICLE OVERLAP 'C' SETTINGS
PHASE: 12345678910111213141516
VEH OVL PARENTS: XX
VEH OVL NOT VEH:
VEH OVL NOT PED:
VEH OVL GRN EXT:
STARTUP COLOR: - RED - YELLOW - GREEN
FLASH COLORS: - RED - YELLOW X GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0=255 SEC)...0
YELLOW CLEAR (0=PARENT.3-25.5 SEC)...0.0
RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0
    ↓
    PRESS '+'
    
```

← NOTICE GREEN FLASH

```

PAGE 1: VEHICLE OVERLAP 'D' SETTINGS
PHASE: 12345678910111213141516
VEH OVL PARENTS: XX
VEH OVL NOT VEH:
VEH OVL NOT PED:
VEH OVL GRN EXT:
STARTUP COLOR: - RED - YELLOW - GREEN
FLASH COLORS: - RED - YELLOW X GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...N
GREEN EXTENSION (0=255 SEC)...0
YELLOW CLEAR (0=PARENT.3-25.5 SEC)...0.0
RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0
    ↓
    PRESS '+'
    
```

← NOTICE GREEN FLASH

OVERLAP PROGRAMMING COMPLETE

FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

1. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
2. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

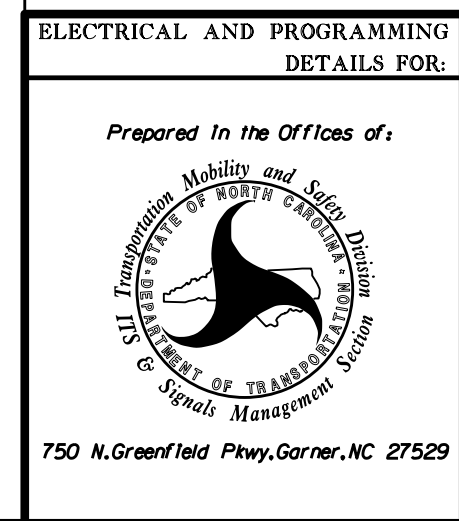
OUTPUT REFERENCE SCHEDULE

USE TO INTERPRET LOGIC PROCESSOR

- OUTPUT 39 = Overlap D Red
- OUTPUT 40 = Overlap D Yellow
- OUTPUT 41 = Overlap D Green
- OUTPUT 42 = Overlap C Red
- OUTPUT 43 = Overlap C Yellow
- OUTPUT 44 = Overlap C Green
- OUTPUT 47 = Overlap B Red
- OUTPUT 48 = Overlap B Yellow
- OUTPUT 49 = Overlap B Green
- OUTPUT 50 = Overlap A Red
- OUTPUT 51 = Overlap A Yellow
- OUTPUT 52 = Overlap A Green

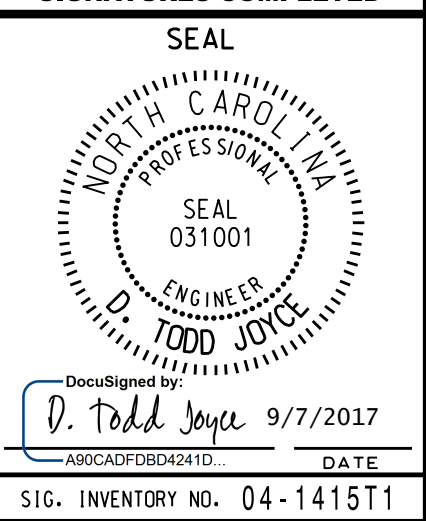
THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 04-1415T1
DESIGNED: August 2017
SEALED: 9/5/2017
REVISED:

Electrical Detail - Temp 1 - Sheet 2 of 2



SR 1923 (Booker Dairy Road) at Kellie Dr/Smithfield-Selma High School	
Division 4	Johnston County
Smithfield	
PLAN DATE: August 2017	REVIEWED BY: T. Joyce
PREPARED BY: C. Strickland	REVIEWED BY:
REVISIONS	INIT. DATE

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



SIG. INVENTORY NO. 04-1415T1

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