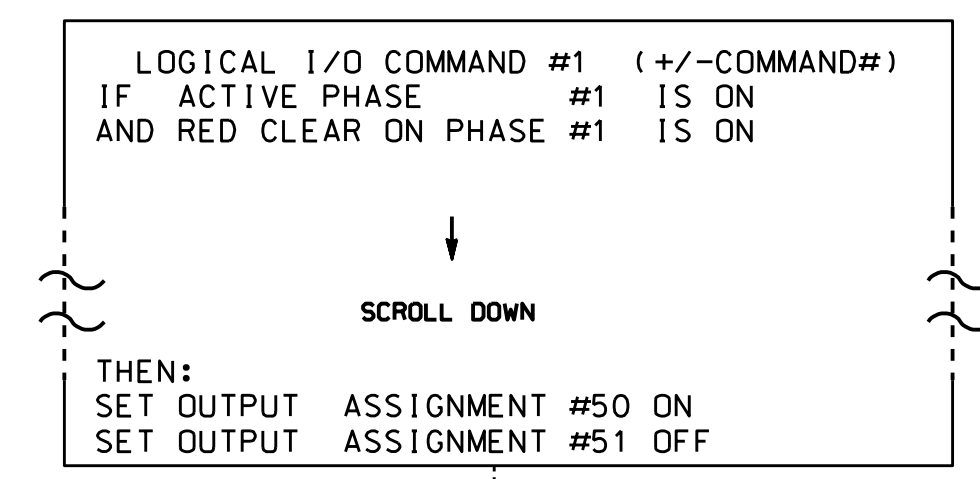


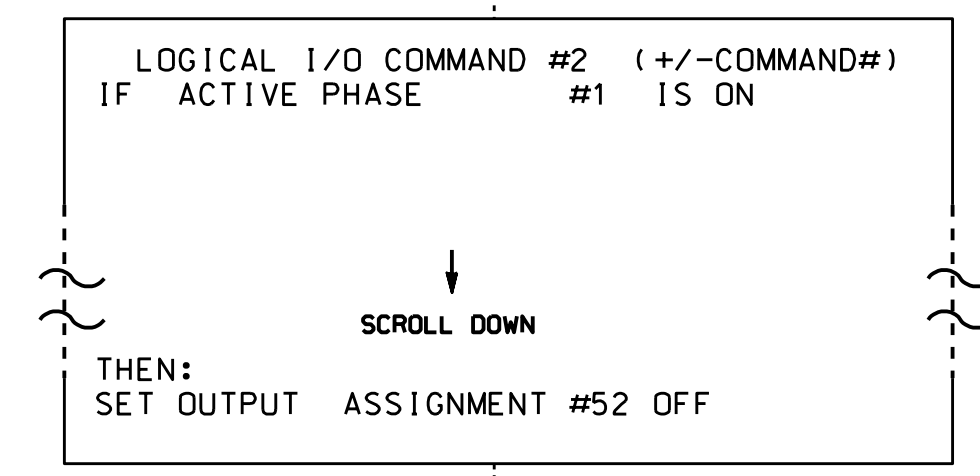
## LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

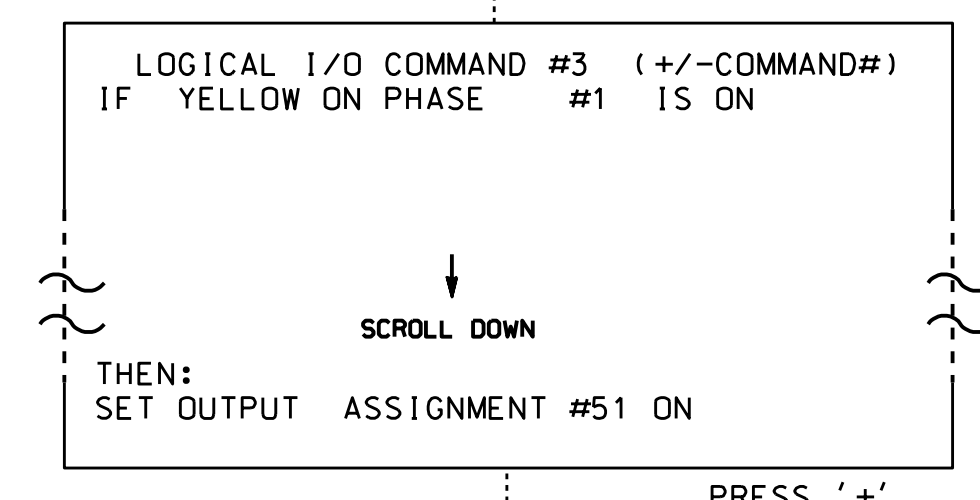
1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, AND 12.
2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



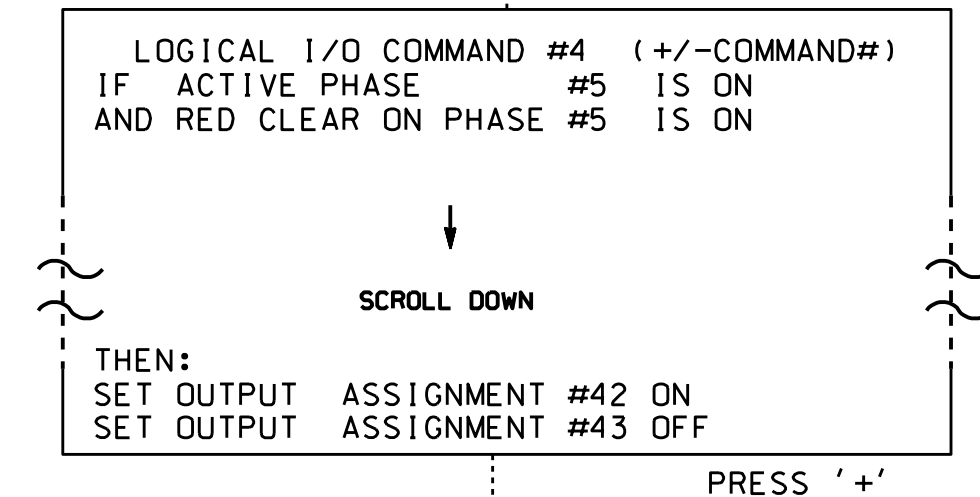
NOTE: LOGIC FOR PHASE 1 RED CLEAR WHEN TRANSITIONING FROM PHASE 1 TO PHASE 2 (HEAD 11).



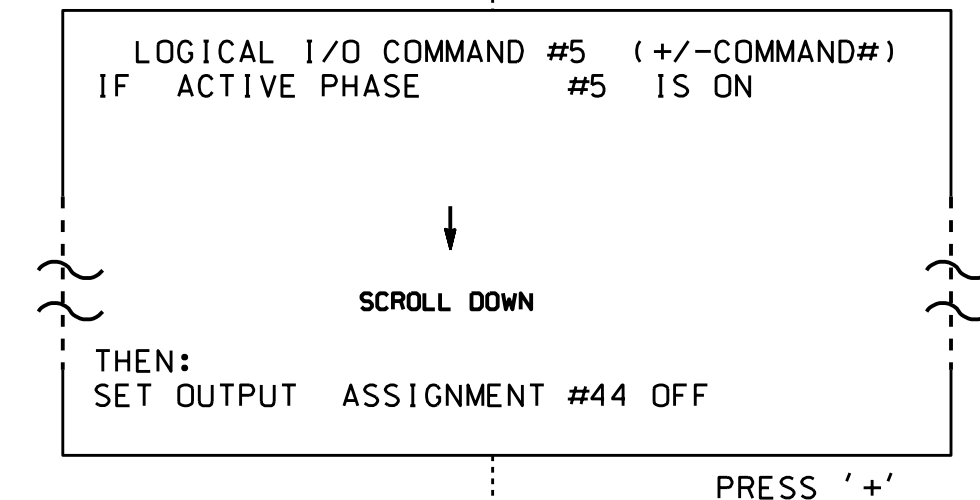
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW OFF DURING PHASE 1 (HEAD 11).



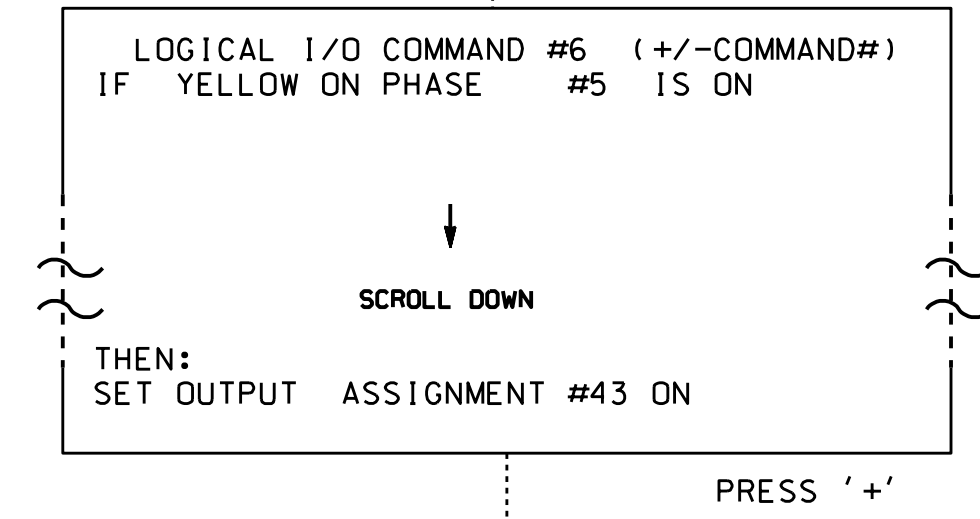
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 1 (HEAD 11).



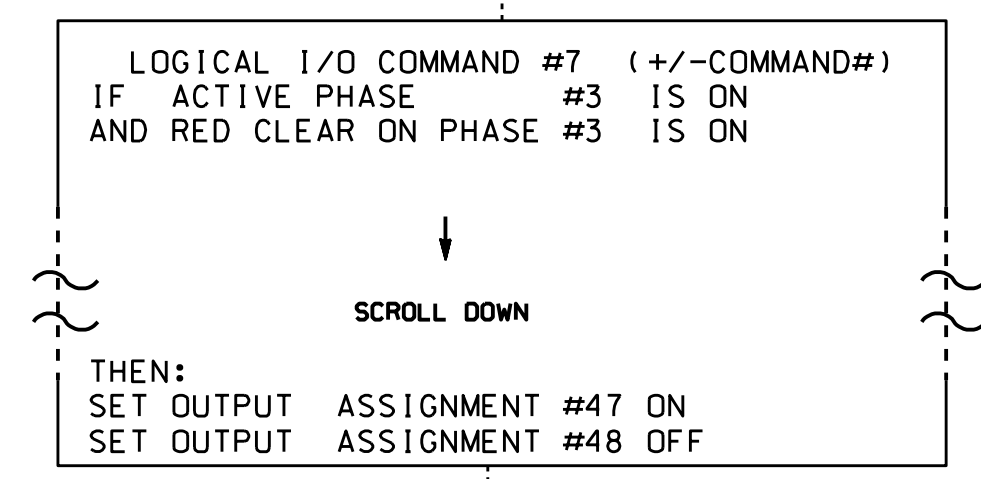
NOTE: LOGIC FOR PHASE 5 RED CLEAR WHEN TRANSITIONING FROM PHASE 5 TO PHASE 6 (HEAD 51).



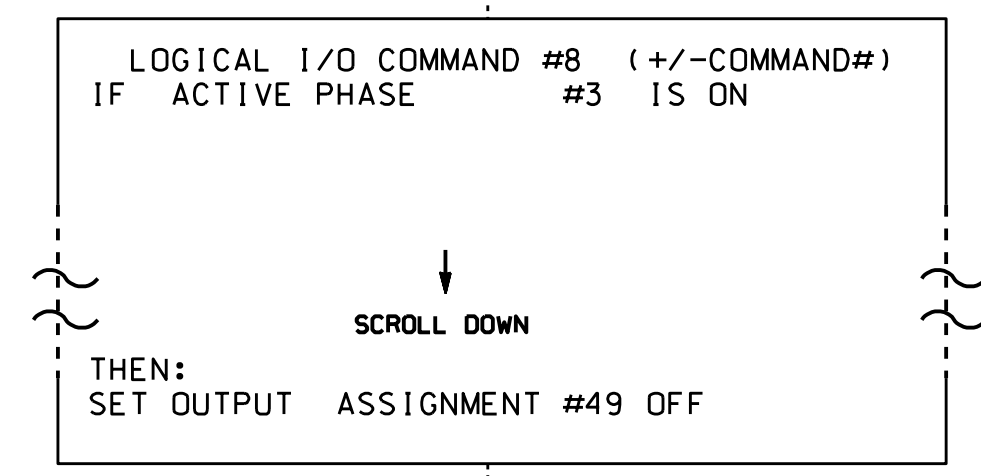
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW OFF DURING PHASE 5 (HEAD 51).



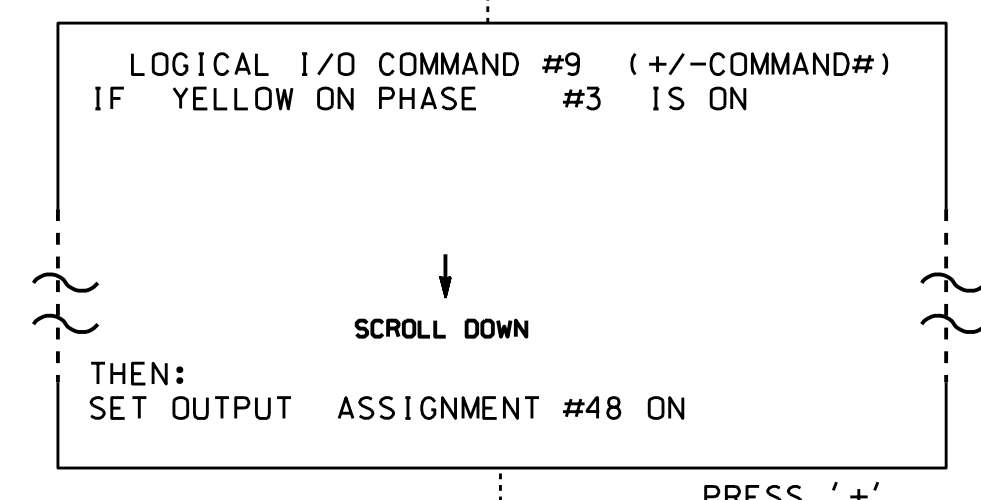
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 5 (HEAD 51).



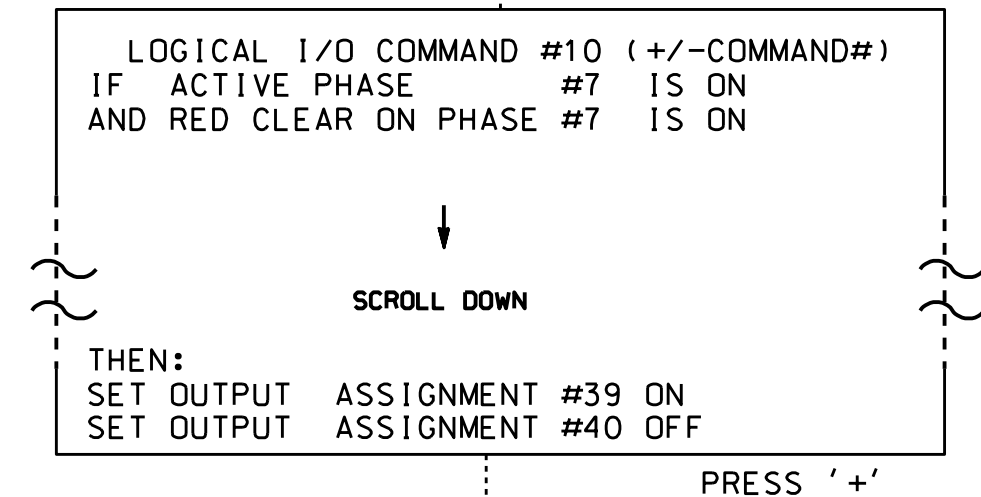
NOTE: LOGIC FOR PHASE 3 RED CLEAR WHEN TRANSITIONING FROM PHASE 3 TO PHASE 4 (HEAD 31).



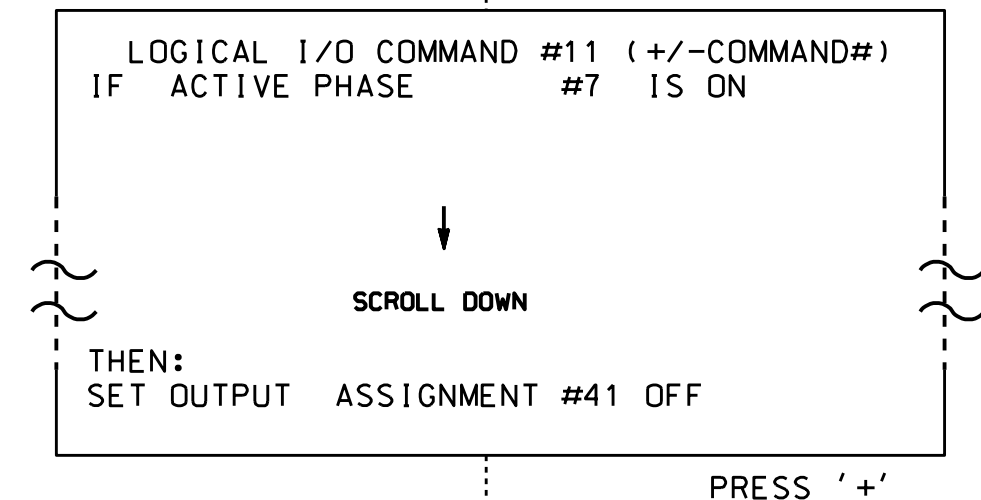
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW OFF DURING PHASE 3 (HEAD 31).



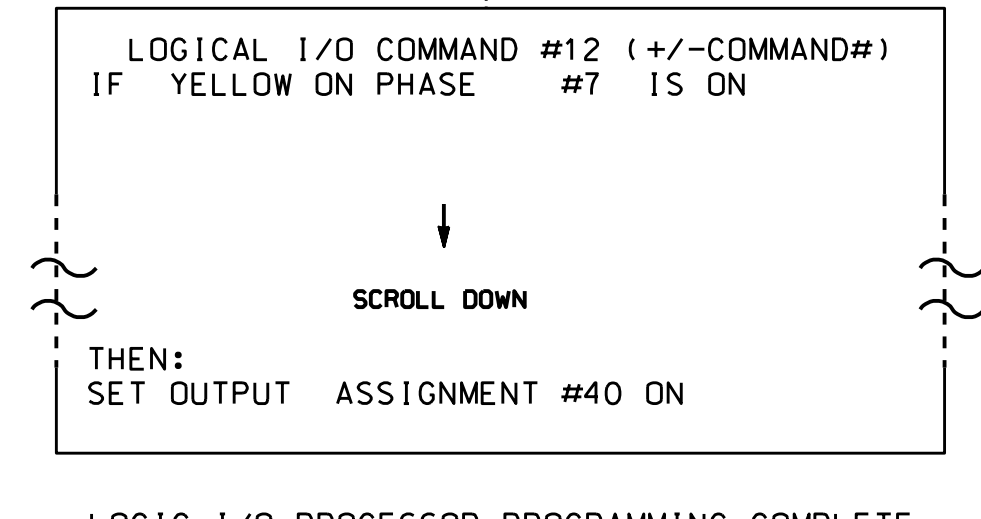
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 3 (HEAD 31).



NOTE: LOGIC FOR PHASE 7 RED CLEAR WHEN TRANSITIONING FROM PHASE 7 TO PHASE 8 (HEAD 71).



NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW OFF DURING PHASE 7 (HEAD 71).



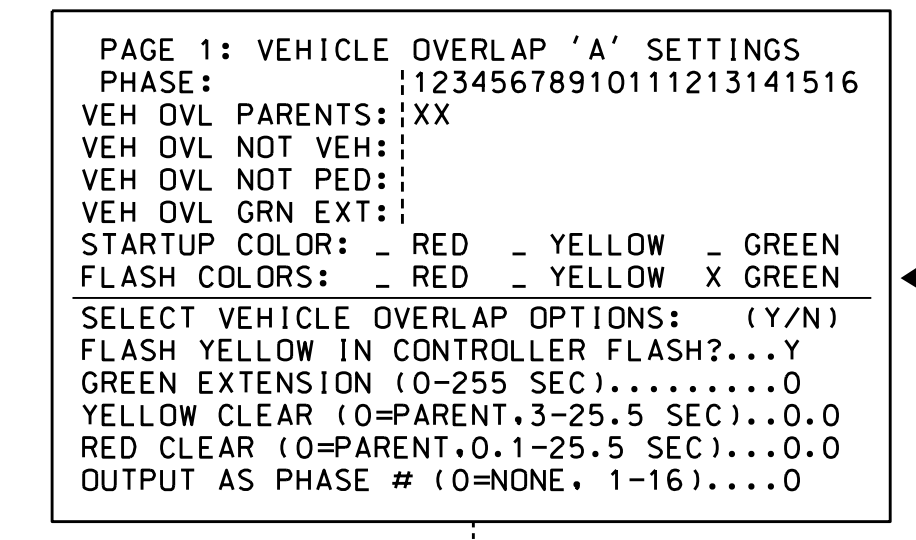
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 7 (HEAD 71).

LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

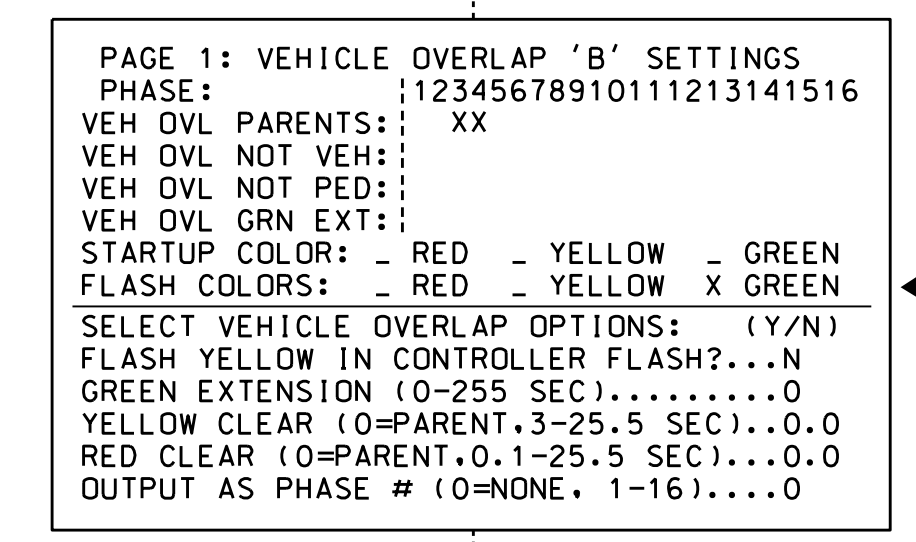
## OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

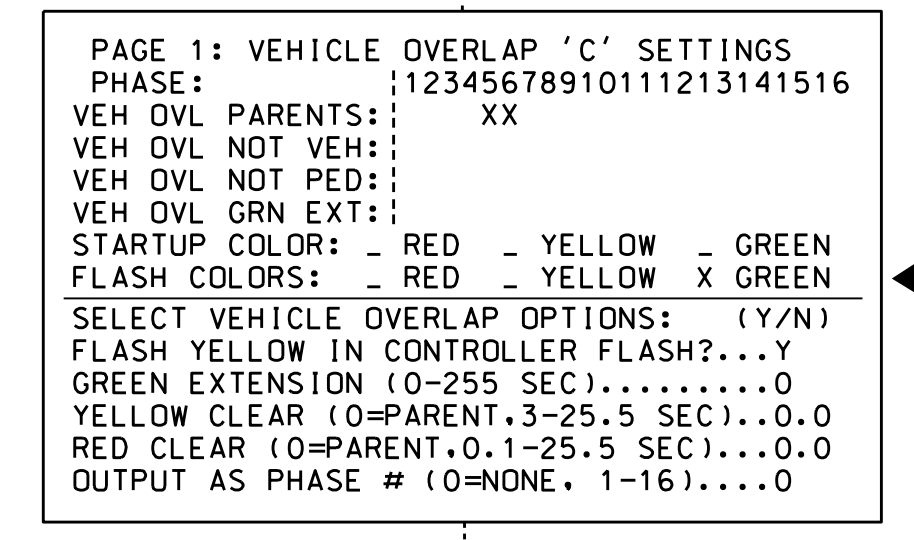
FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).



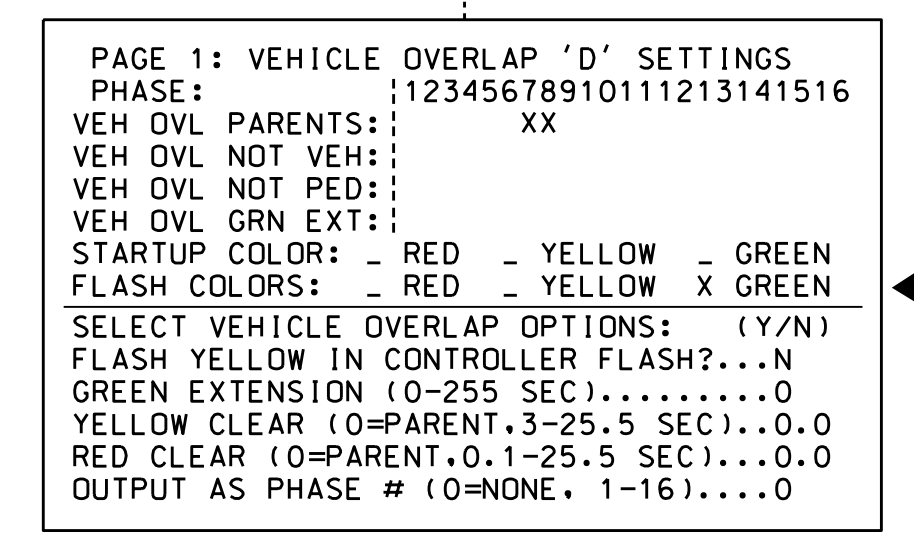
PRESS '+'



PRESS '+'



PRESS '+'



OVERLAP PROGRAMMING COMPLETE

## FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

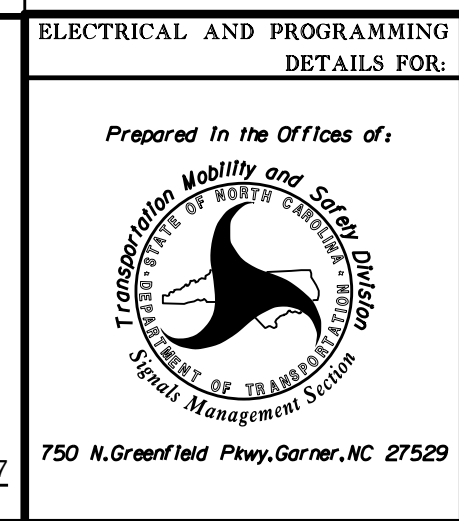
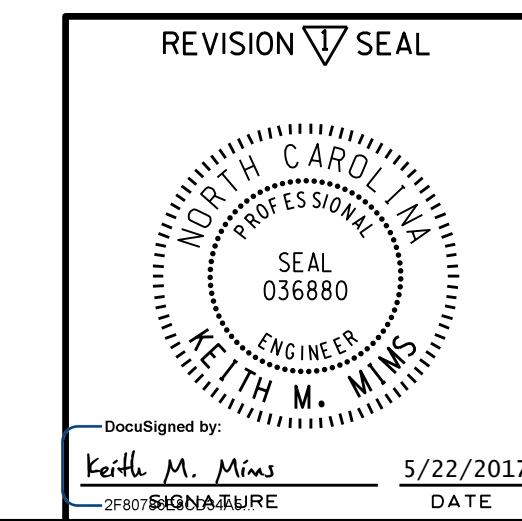
1. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
2. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

<b>OUTPUT REFERENCE SCHEDULE</b>	
USE TO INTERPRET LOGIC PROCESSOR	
OUTPUT 39 =	Overlap D Red
OUTPUT 40 =	Overlap D Yellow
OUTPUT 41 =	Overlap D Green
OUTPUT 42 =	Overlap C Red
OUTPUT 43 =	Overlap C Yellow
OUTPUT 44 =	Overlap C Green
OUTPUT 47 =	Overlap B Red
OUTPUT 48 =	Overlap B Yellow
OUTPUT 49 =	Overlap B Green
OUTPUT 50 =	Overlap A Red
OUTPUT 51 =	Overlap A Yellow
OUTPUT 52 =	Overlap A Green

THIS ELECTRICAL DETAIL IS FOR  
THE SIGNAL DESIGN: 03-0824  
DESIGNED: March 2017  
SEALED: 5-12-17  
REVISED: N/A

Electrical Detail - Sheet 2 of 2



NC 904/NC 179 - 904 (Seaside Rd) at NC 179/SR 1163 (Old Georgetown Rd)	
Division 3	Brunswick County
PLAN DATE: June 2009	REVIEWED BY: R. Hinshaw
PREPARED BY: K. Moore	REVIEWED BY:
REVISIONS	DATE
Changed head 42 to a 3-section head, added Note 8 and eliminated loop 4C. (KMM)	5/22/2017

**DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED**

Not a certified document as to the Original Document but only as to the Revisions - This document originally issued and sealed by F. Royal Hinshaw, PE #032117, on 7-27-09. This document is only certified as to the revisions.

SIG. INVENTORY NO. 03-0824

2017-05-17 13:59 C:\MTSAS\0415\Sig\Signal\work\log\output\sig\Main\Refer\sem\030824\_sml.ele\_20170517.dgn T:\peter@son