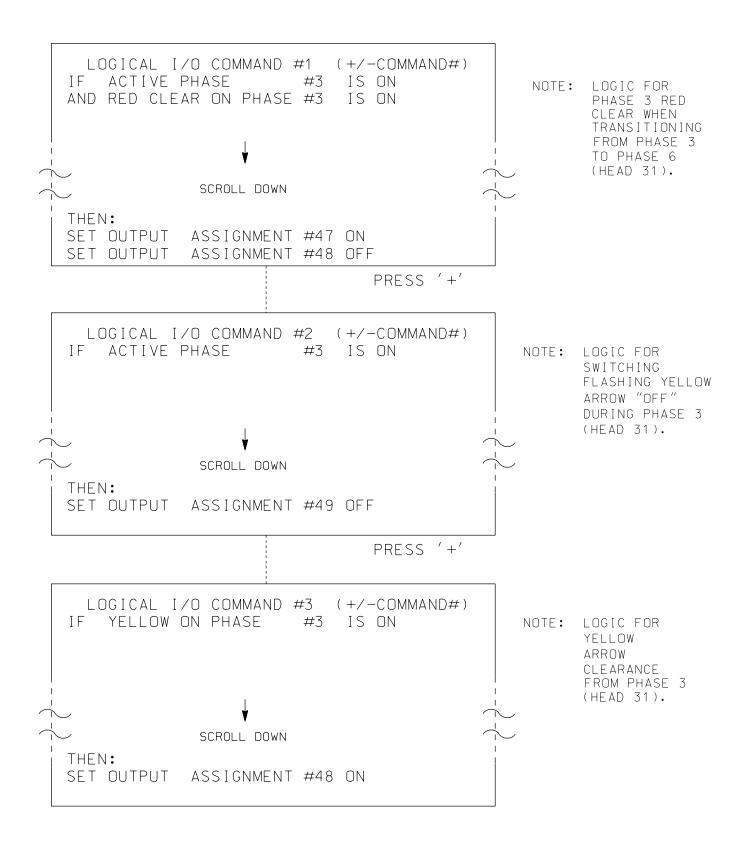
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OUTPUT REFERENCE SCHEDULE USE TO INTERPRET LOGIC PROCESSOR OUTPUT 47 = Overlap B Red OUTPUT 48 = Overlap B Yellow OUTPUT 49 = Overlap B Green

OVERLAP PROGRAMMING DETAIL FOR DEFAULT PHASING

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

PRESS '+'



OVERLAP PROGRAMMING COMPLETE

OVERLAP PROGRAMMING DETAIL FOR ALTERNATE PHASING

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS). PRESS 'NEXT' TO ADVANCE TO PAGE 2.

PRESS '+'

PAGE 2

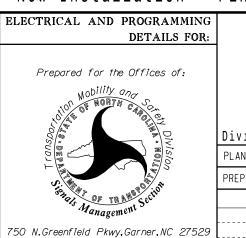
PAGE 2: VEHICLE OVERLAP 'B' SETTINGS | 12345678910111213141516 PHASE: VEH OVL PARENTS: X VEH OVL NOT VEH: | VEH OVL NOT PED: | VEH OVL GRN EXT: STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW _ GREEN SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?...Y GREEN EXTENSION (0-255 SEC)..... YELLOW CLEAR (O=PARENT,3-25.5 SEC)..0.0 RED CLEAR (0=PARENT, 0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: Ø3-11Ø4 DESIGNED: April 2017 SEALED: REVISED:

DOCUMENT NOT CONSIDERED FINAL **UNLESS ALL SIGNATURES COMPLETED**

New Installation - Final Design (Electrical Detail Sheet 2 of 4)



Southbound SR 1409 (Military Cutoff Road)

Brittany Lakes Road Division 03 New Hanover County Wilmi<u>ngton</u>! PLAN DATE: April 2017 REVIEWED BY: MB Toth

PREPARED BY: AM Encarnacion | REVIEWED BY: REVISIONS INIT. DATE

6/6/2017 Melissa B. Toth SIG. INVENTORY NO. 03-1104

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025892

SEAL