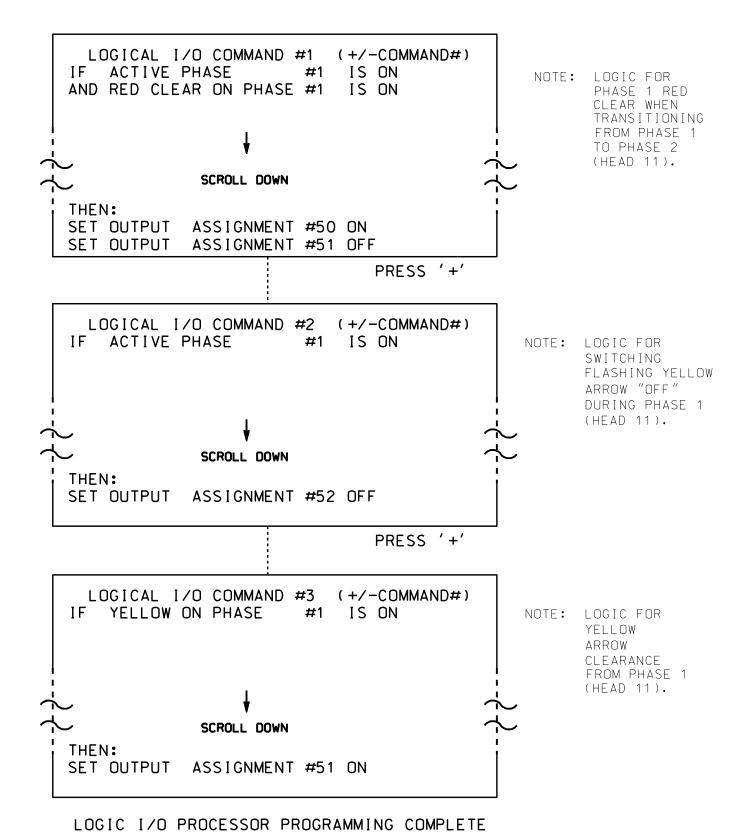
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



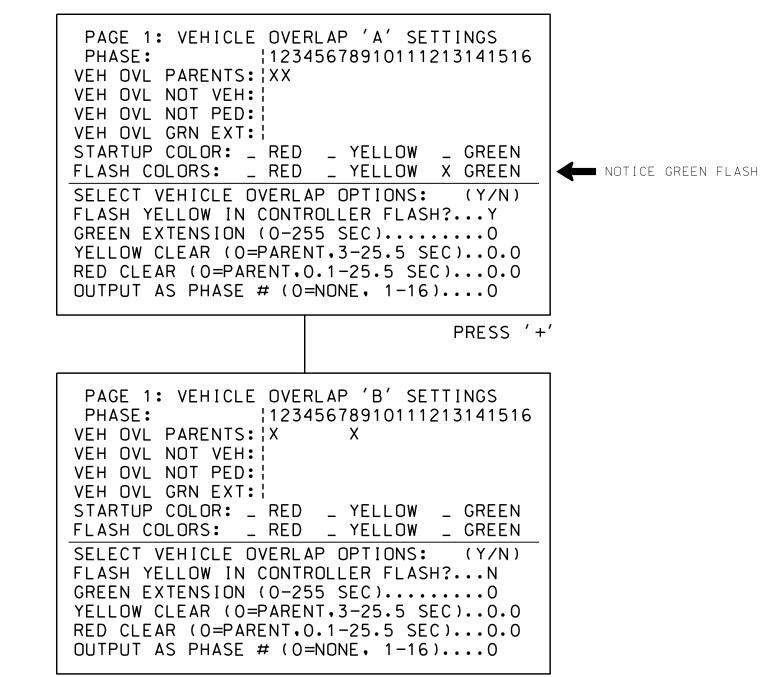
OUTPUT REFERENCE SCHEDULE

OUTPUT 50 = Overlap A Red OUTPUT 51 = Overlap A Yellow OUTPUT 52 = Overlap A Green

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

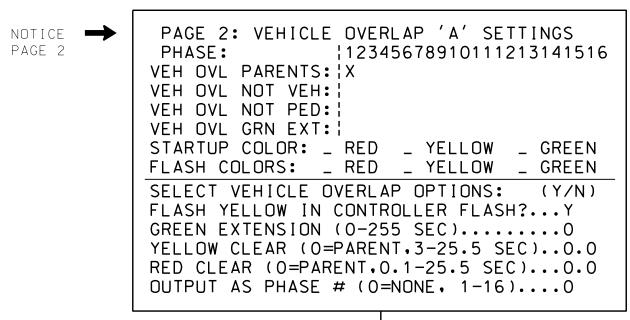


OVERLAP PROGRAMMING COMPLETE

OVERLAP PROGRAMMING DETAIL FOR ALTERNATE PHASING - PAGE 2

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS). THEN '1' (VEHICLE OVERLAP SETTINGS). PRESS 'NEXT' TO ADVANCE TO PAGE 2.



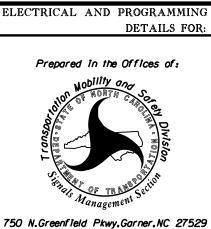
PRESS '+'

PAGE 2: VEHICLE OVERLAP 'B' SETTINGS PHASE: 12345678910111213141516 VEH OVL PARENTS: X VEH OVL NOT VEH: | VEH OVL NOT PED: VEH OVL GRN EXT: | STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW _ GREEN SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?...N GREEN EXTENSION (0-255 SEC)...... YELLOW CLEAR (O=PARENT,3-25.5 SEC)..0.0 RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

OVERLAP PROGRAMMING COMPLETE

Electrical Detail - Sheet 2 of 4

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 09-0511 DESIGNED: April 2017 SEALED: 5/16/2017 REVISED:



PAGE 2

US 158 (Reidsville Road) I-74 WB Ramps

ivision 9 Forsvth Countv Winston-Salem PLAN DATE: May 2017 REVIEWED BY:

T. Joyce PREPARED BY: C. Strickland | REVIEWED BY: REVISIONS INIT. DATE

SIG. INVENTORY NO. 09-0511

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL

SIGNATURES COMPLETED

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