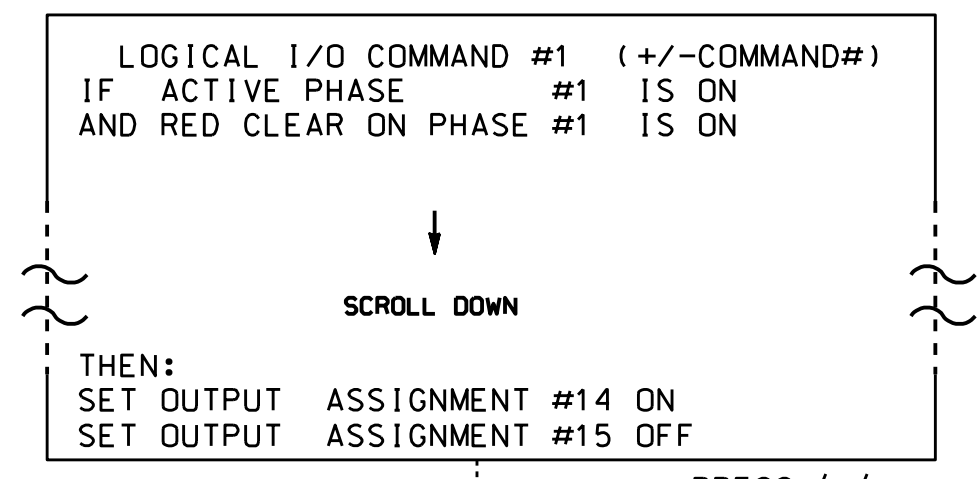


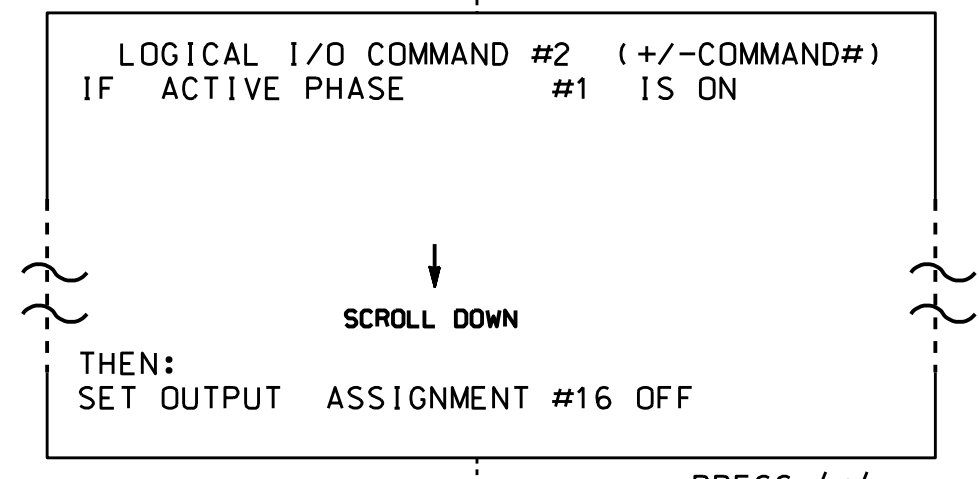
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

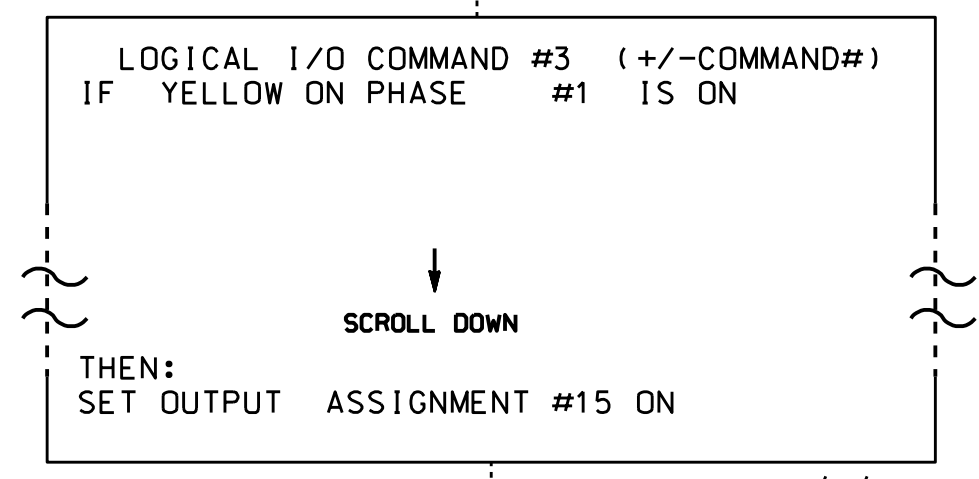
1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, and 12.
2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



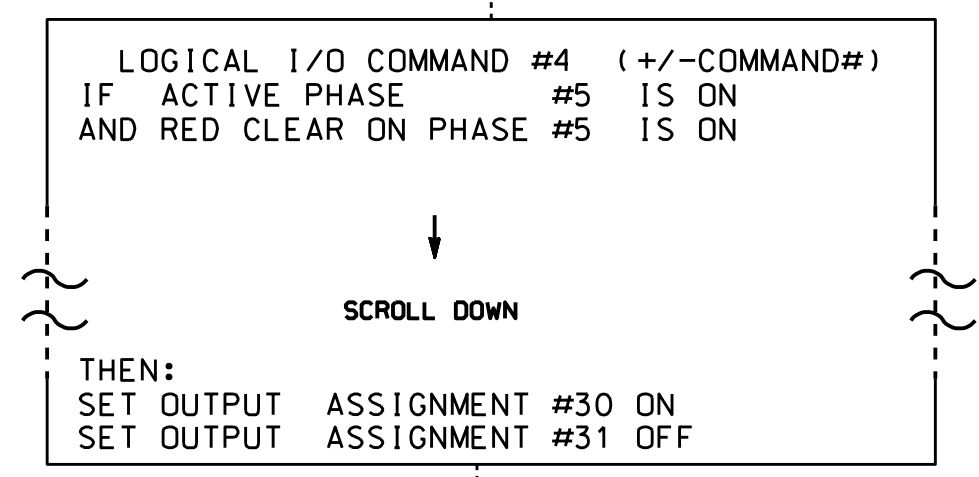
NOTE: LOGIC FOR PHASE 1 RED CLEAR WHEN TRANSITIONING FROM PHASE 1 TO PHASE 2 (HEAD 11).



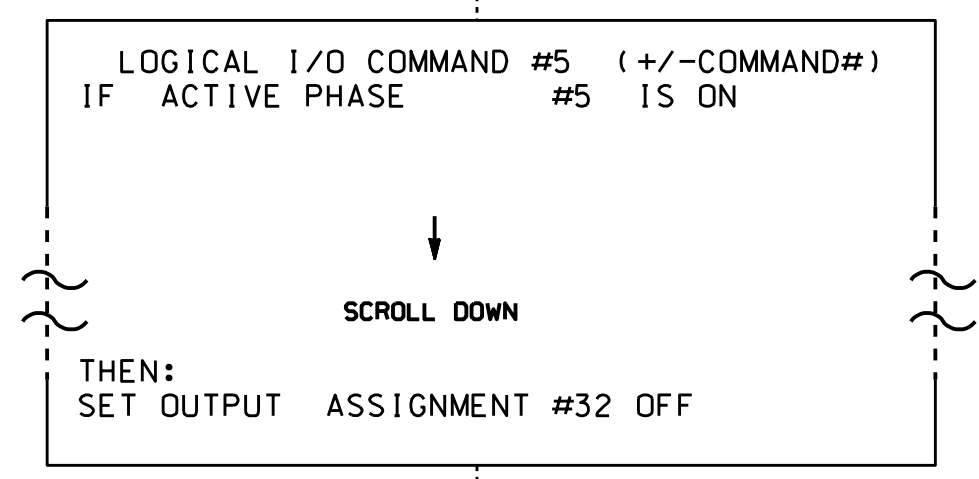
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 1 (HEAD 11).



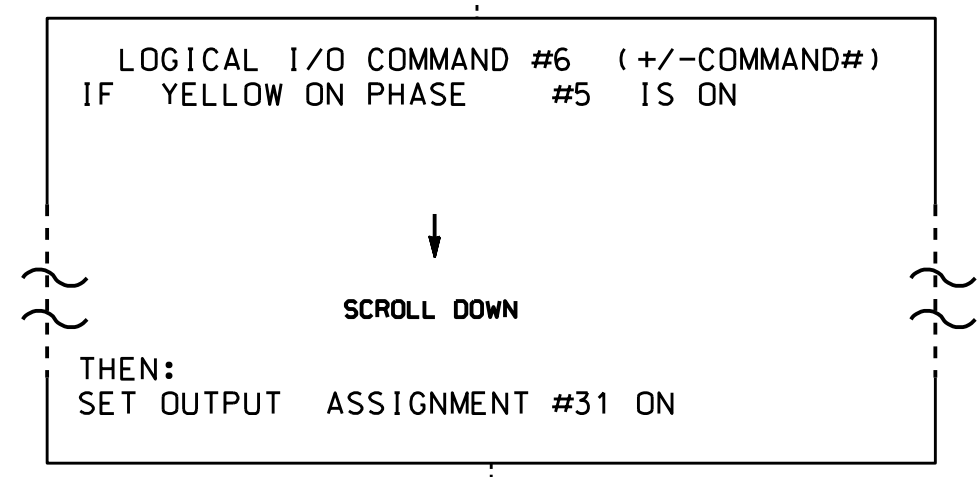
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 1 (HEAD 11).



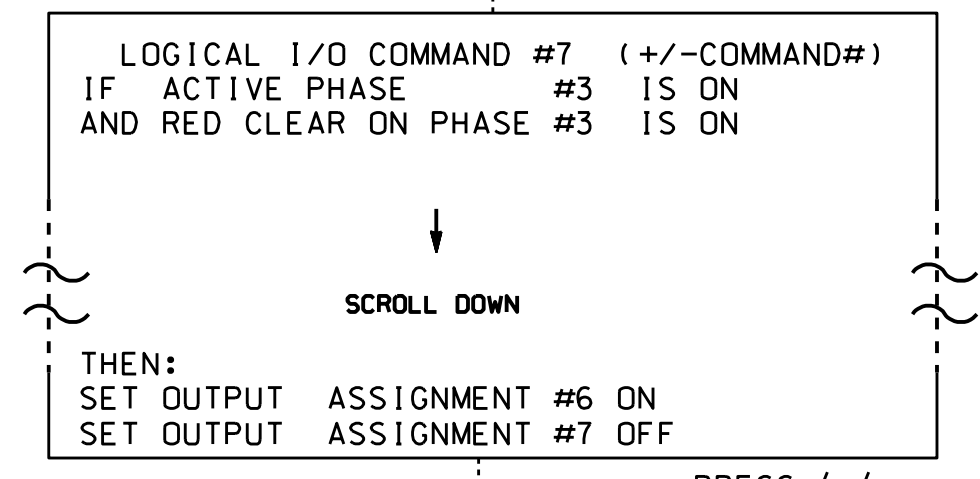
NOTE: LOGIC FOR PHASE 5 RED CLEAR WHEN TRANSITIONING FROM PHASE 5 TO PHASE 6 (HEAD 51).



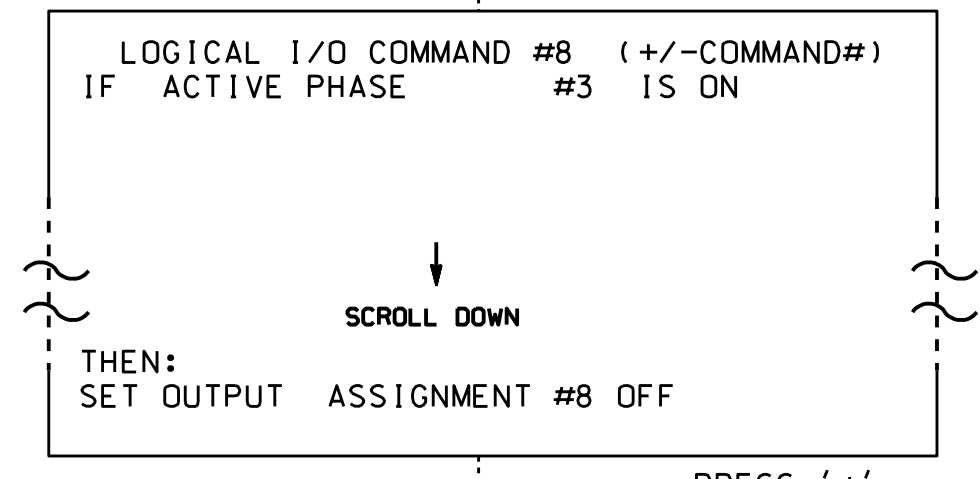
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 5 (HEAD 51).



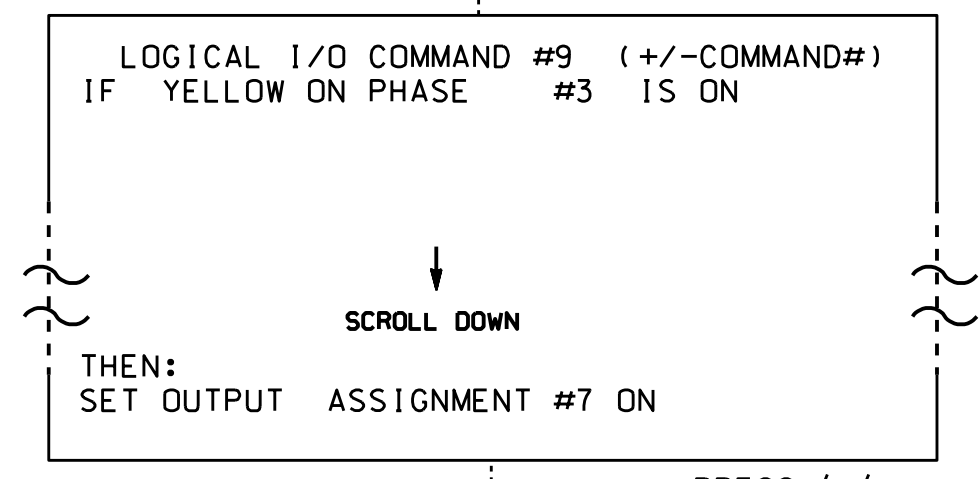
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 5 (HEAD 51).



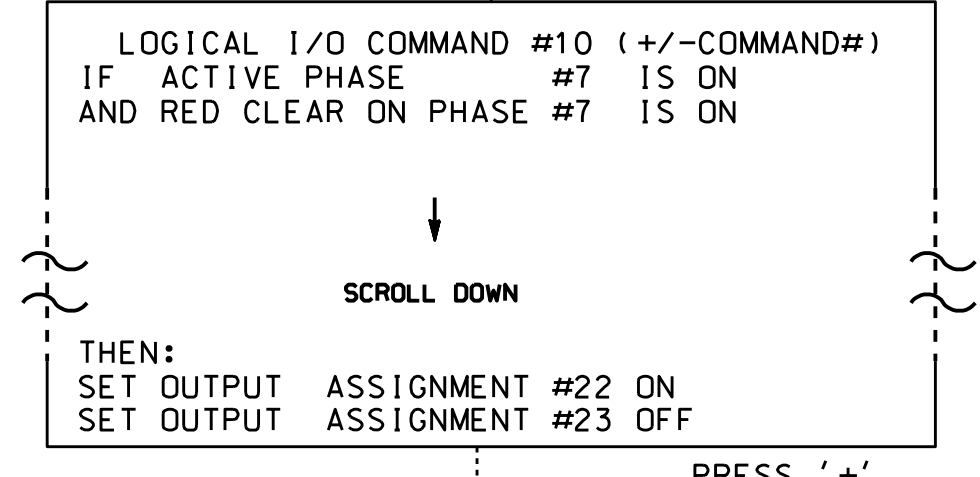
NOTE: LOGIC FOR PHASE 3 RED CLEAR WHEN TRANSITIONING FROM PHASE 3 TO PHASE 4 (HEAD 31).



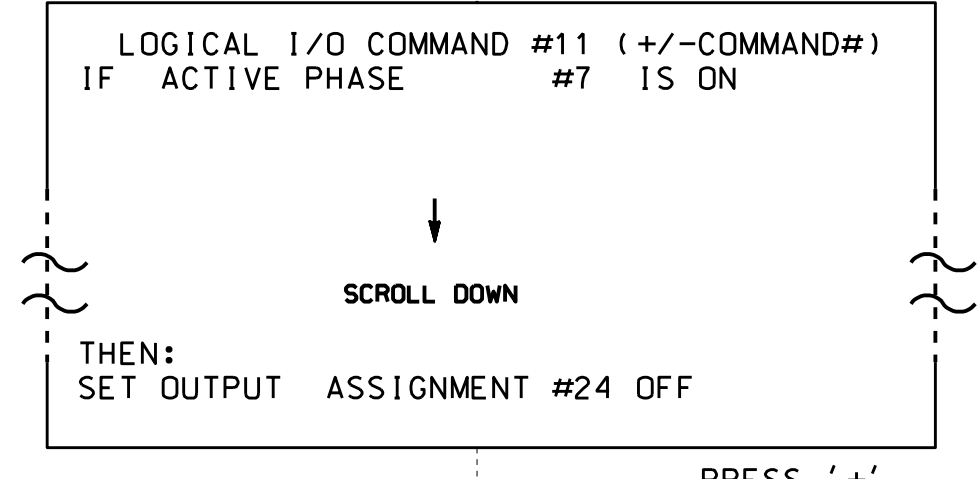
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 3 (HEAD 31).



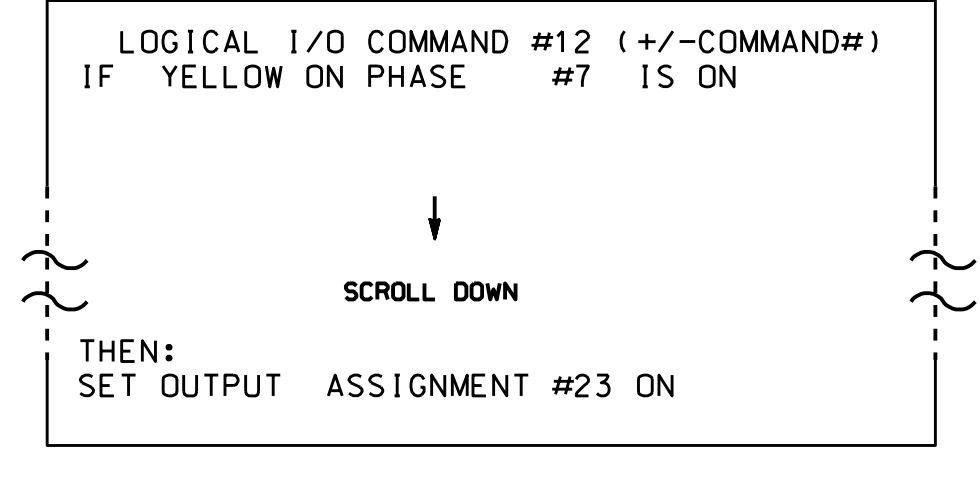
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 3 (HEAD 31).



NOTE: LOGIC FOR PHASE 7 RED CLEAR WHEN TRANSITIONING FROM PHASE 7 TO PHASE 8 (HEAD 71).



NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 7 (HEAD 71).



NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 7 (HEAD 71).

OUTPUT REFERENCE SCHEDULE

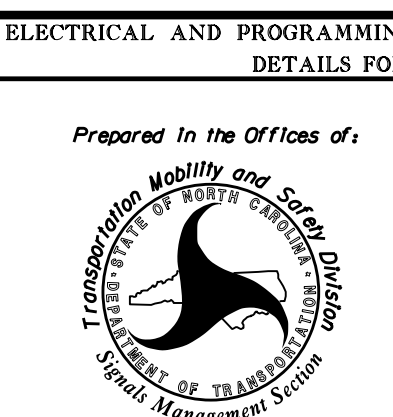
- OUTPUT 14 = Overlap A Red
- OUTPUT 15 = Overlap A Yellow
- OUTPUT 16 = Overlap A Green
- OUTPUT 6 = Overlap B Red
- OUTPUT 7 = Overlap B Yellow
- OUTPUT 8 = Overlap B Green
- OUTPUT 30 = Overlap C Red
- OUTPUT 31 = Overlap C Yellow
- OUTPUT 32 = Overlap C Green
- OUTPUT 22 = Overlap D Red
- OUTPUT 23 = Overlap D Yellow
- OUTPUT 24 = Overlap D Green
- OUTPUT 33 = Phase 1 Green
- OUTPUT 34 = Phase 5 Green
- OUTPUT 35 = Phase 3 Green
- OUTPUT 36 = Phase 7 Green

Note: All outputs shown above have been remapped. See sheets 4 through 7 of this electrical detail.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 12-0596T
DESIGNED: January 2017
SEALED: 2/20/2017
REVISED:

06-MAR-2017 14:17 C:\MTS\SIG\12-0596T\SIG\12-0596T.dgn

Electrical Detail - Temporary Design - Sheet 3 of 7

	<p>NC 150 (Cherryville Rd.) at NC 180 (North Post Rd.)</p>	<p>SEAL NORTH CAROLINA PROFESSIONAL ENGINEER SEAL 030530 JACOBARY M. LITTLE</p>
Prepared in the Offices of: 750 N. Greenfield Pkwy, Garner, NC 27529	Division 12 Cleveland County Shelby PLAN DATE: February 2017 REVIEWED BY: T. Joyce PREPARED BY: C. Strickland REVIEWED BY:	Documented by: Zachary M. Little 3/7/2017 DATE:
DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED		

LOGIC I/O PROCESSOR PROGRAMMING COMPLETE