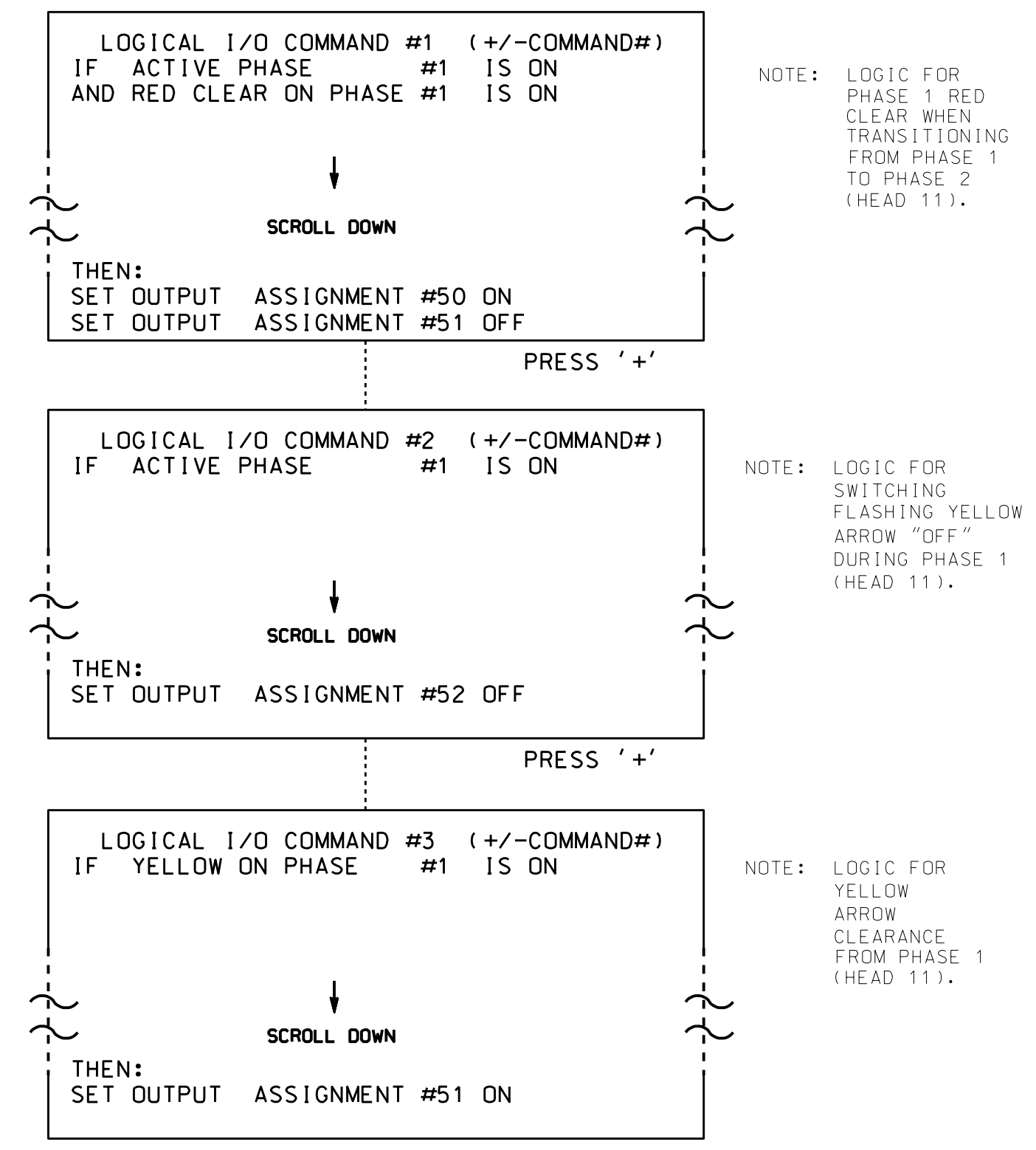


**LOGICAL I/O PROCESSOR PROGRAMMING DETAIL
TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE**

(program controller as shown below)

- FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS), SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
- FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OUTPUT REFERENCE SCHEDULE

OUTPUT 50 = Overlap A Red
OUTPUT 51 = Overlap A Yellow
OUTPUT 52 = Overlap A Green

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

```


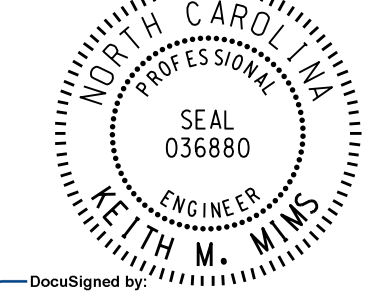
PAGE 1: VEHICLE OVERLAP 'A' SETTINGS
PHASE:      12345678910111213141516
VEH OVL PARENTS: XX
VEH OVL NOT VEH:
VEH OVL NOT PED:
VEH OVL GRN EXT:
STARTUP COLOR:  _ RED  _ YELLOW  _ GREEN
FLASH COLORS:  _ RED  _ YELLOW X GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0-255 SEC).....0
YELLOW CLEAR (0=PARENT,3-25.5 SEC)..0.0
RED CLEAR (0=PARENT,0.1-25.5 SEC)..0.0
OUTPUT AS PHASE # (0=NONE, 1-16)....0
    
```

← NOTICE GREEN FLASH

OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 07-2132
DESIGNED: November 2016
SEALED: 1/24/2017
REVISED: N/A

25-Jan-2017 08:48
S:\ITS\SSU\ITS_Signals\workgroups\Sig_Mgmt\armstrong072132_sm.ele.xxx.dgn
sarmstrong

Electrical Detail - Final Design - Sheet 2 of 2		DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED
ELECTRICAL AND PROGRAMMING DETAILS FOR: Prepared In the Offices of: 	SR 1962 (S. Third Street) at SR 1980 (Holmes Road)	SEAL 
	Division 7 Alamance County Mebane PLAN DATE: January 2017 REVIEWED BY: BAS PREPARED BY: S. Armstrong REVIEWED BY:	REVISIONS INIT. DATE