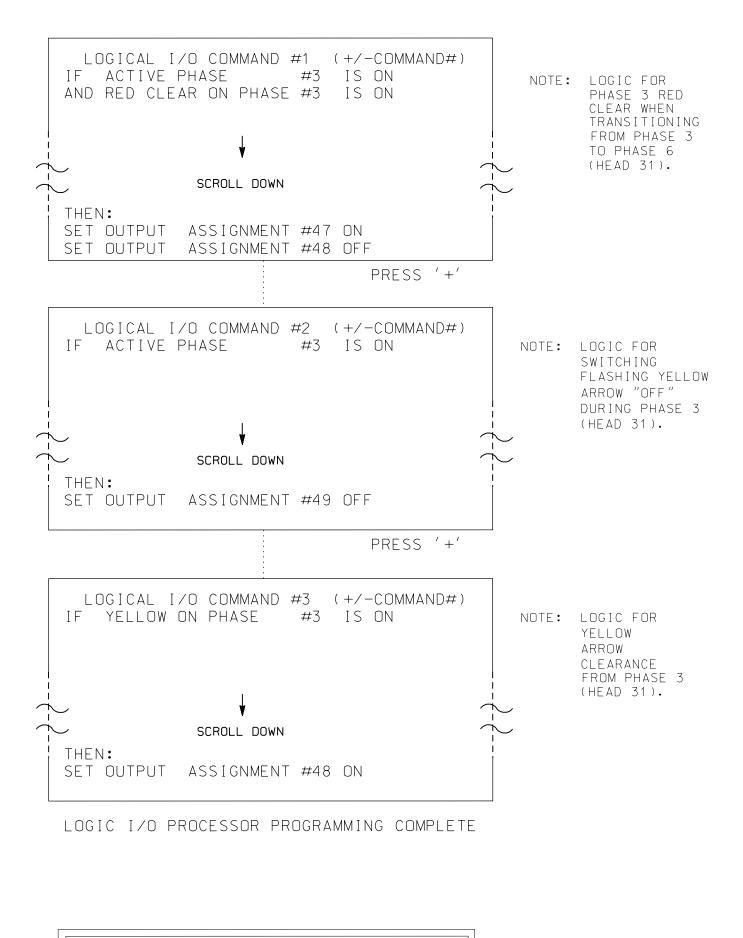
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, and 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



OUTPUT REFERENCE SCHEDULE USE TO INTERPRET LOGIC PROCESSOR OUTPUT 47 = Overlap B Red OUTPUT 48 = Overlap B Yellow OUTPUT 49 = Overlap B Green

COUNTDOWN PEDESTRIAN SIGNAL OPERATION

Countdown Ped Signals are required to display timing only during Ped Clearance Interval. Consult Ped Signal Module user's manual for instructions on selecting this feature.

OVERLAP PROGRAMMING DETAIL FOR DEFAULT PHASING (program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN

'1' (VEHICLE OVERLAP SETTINGS). PRESS '+' PAGE 1: VEHICLE OVERLAP 'B' SETTINGS | 12345678910111213141516 PHASE: VEH OVL PARENTS: X X VEH OVL NOT VEH: | VEH OVL NOT PED: | VEH OVL GRN EXT: STARTUP COLOR: _ RED _ YELLOW _ GREEN NOTICE GREEN FLASH FLASH COLORS: _ RED _ YELLOW X GREEN SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?...Y GREEN EXTENSION (0-255 SEC)..... YELLOW CLEAR (O=PARENT,3-25.5 SEC)..0.0 RED CLEAR (0=PARENT,0.1-25.5 SEC)...0.0

OVERLAP PROGRAMMING COMPLETE

OUTPUT AS PHASE # (0=NONE, 1-16)...0

OVERLAP PROGRAMMING DETAIL FOR ALTERNATE PHASING

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS). PRESS NEXT TO ADVANCE TO PAGE 2.

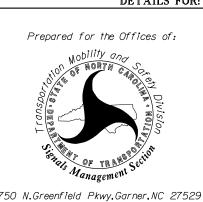
PRESS '+' NOTICE PAGE 2 PAGE 2: VEHICLE OVERLAP 'B' SETTINGS 12345678910111213141516 PHASE: VEH OVL PARENTS: X VEH OVL NOT VEH: | VEH OVL NOT PED: | VEH OVL GRN EXT: 1 STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW _ GREEN SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?...Y GREEN EXTENSION (0-255 SEC)..... YELLOW CLEAR (O=PARENT,3-25.5 SEC)..0.0 RED CLEAR (0=PARENT, 0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 10-2195 DESIGNED: June 2015 SEALED: August 30, 2016 REVISED:

| ELECTRICAL DETAIL SHEET 2 OF 4

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



PROGRAMMING DETAILS FOR: US 74 (Andrew Jackson Highway) Westbound Division 10

SR 1515 (Sardis Church Road) Union County

Indian Trai PLAN DATE: June 2015 REVIEWED BY: L Moon PREPARED BY: K Smith REVIEWED BY: B Humfleet REVISIONS

022516 SIG. INVENTORY NO. 10-2195

PLANS PREPARED BY:

DRMP, INC. 5950 FAIRVIEW ROAD, SUITE 320 CHARLOTTE, NC 28210 NC LICENSE NO. C-2213 • (704) 332-2289