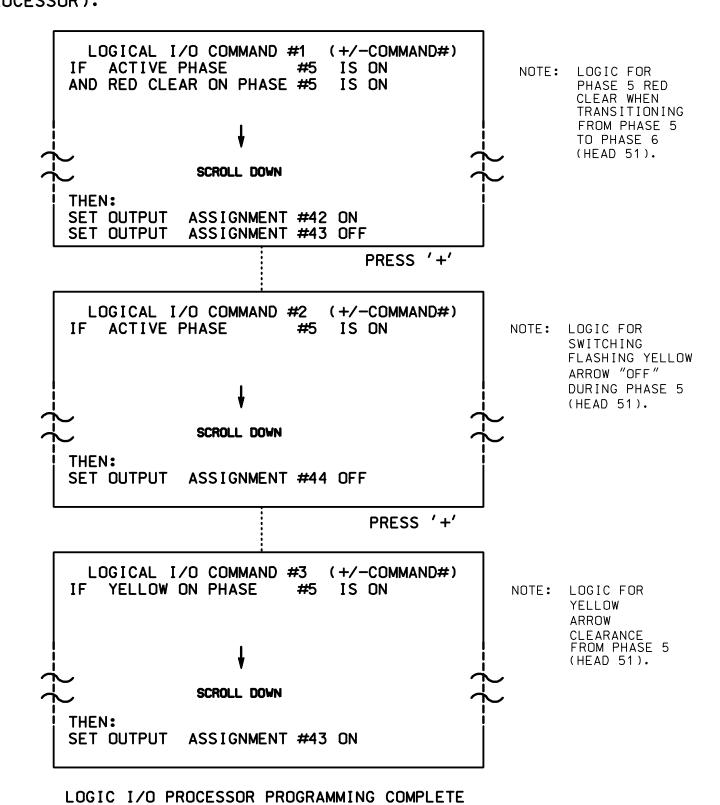
PROJECT REFERENCE NO. I-5000

LOGICAL I/O PROCESSOR PROGRAMMING DETAIL

TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



OUTPUT REFERENCE SCHEDULE

OUTPUT 42 = Overlap C Red OUTPUT 43 = Overlap C Yellow OUTPUT 44 = Overlap C Green

OVERLAP PROGRAMMING DETAIL FOR DEFAULT PHASING

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

PRESS '+' TWICE

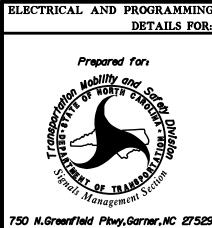
PAGE 1: VEHICLE OVERLAP 'C' SETTINGS 12345678910111213141516 PHASE: VEH OVL PARENTS: | XX VEH OVL NOT VEH: VEH OVL NOT PED: VEH OVL GRN EXT: | STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW X GREEN NOTICE GREEN FLASH SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?...Y GREEN EXTENSION (0-255 SEC).....0 YELLOW CLEAR (O=PARENT,3-25.5 SEC)..0.0 RED CLEAR (0=PARENT, 0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 12-1623T1 DESIGNED: September 2016 SEALED: 11-08-2016 REVISED:

Temporary Signal - Phase 1, Step 1 (Sheet 2 of 2)

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



US 321 (N. Chester Street)

Radio Street Division 12

Gaston Co. Gastonia PLAN DATE: September 2016 REVIEWED BY: T.R. Terrell PREPARED BY: J.A. Wagner REVIEWED BY: N.R. Simmons INIT. DATE REVISIONS

SIG. INVENTORY NO. 12-1623T

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