PROJECT REFERENCE NO.	SHEET NO.
U-5742	Sig. 42.3

ECONOLITE ASC/3-2070 LOGIC PROCESSOR PROGRAMMING DETAIL

(program controller as shown)

1. From Main Menu select **1. CONFIGURATION**

2. From CONFIGURATION Submenu select **8. LOGIC PROCESSOR**

3. From the LOGIC PROCESSOR Submenu select **2. LOGIC STATEMENTS**

ENTER A "1" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:   1  COPY FROM:   1  ACTIVE:  M   FALSE
IF     CTR PHASE TIMING      1     IS  ON

THEN   SIG SET OVLP GREEN    1        OFF


ELSE
```

LOGIC FOR TURNING FLASHING YELLOW ARROW OFF DURING PHASE 1 (HEADS 83.84)

ENTER A "2" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:   2  COPY FROM:   2  ACTIVE:  M   FALSE
IF     VEH YELLOW ON PH      1     IS  ON

THEN   SIG SET OLP YELLOW    1        ON


ELSE
```

LOGIC FOR YELLOW ARROW CLEARANCE WHEN LEAVING PHASE 1 (HEADS 83.84)

ENTER A "3" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:   3  COPY FROM:   3  ACTIVE:  M   FALSE
IF     CTR PHASE TIMING      1     IS  ON
AND    VEH RED ON PHASE      1     IS  ON

THEN   SIG SET OLP RED       1        ON


ELSE
```

LOGIC FOR RED SIGNAL CLEARANCE WHEN LEAVING PHASE 1 (HEADS 83.84)

ENTER A "4" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:   4  COPY FROM:   4  ACTIVE:  M   FALSE
IF     VEH OVERLAP           7     IS  ON

THEN   SIG SET OVLP GREEN    2        OFF


ELSE
```

LOGIC FOR TURNING FLASHING YELLOW ARROW OFF DURING OLG. WHICH HAS PARENT PHASE 7 (HEAD 64)

ENTER A "5" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:   5  COPY FROM:   5  ACTIVE:  M   FALSE
IF     VEH OVERLAP YLW       7     IS  ON

THEN   SIG SET OLP YELLOW    2        ON


ELSE
```

LOGIC FOR YELLOW ARROW CLEARANCE WHEN LEAVING OLG. WHICH HAS PARENT PHASE 7 (HEAD 64)

ENTER A "6" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:   6  COPY FROM:   6  ACTIVE:  M   FALSE
IF     VEH OVERLAP           7     IS  ON
AND    VEH OVERLAP RED       7     IS  ON

THEN   SIG SET OLP RED       2        ON


ELSE
```

LOGIC FOR RED SIGNAL CLEARANCE WHEN LEAVING OLG. WHICH HAS PARENT PHASE 7 (HEAD 64)

ENTER A "7" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:   7  COPY FROM:   7  ACTIVE:  M   FALSE
IF     CTR PHASE TIMING      5     IS  ON

THEN   SIG SET OVLP GREEN    3        OFF


ELSE
```

LOGIC FOR TURNING FLASHING YELLOW ARROW OFF DURING PHASE 5 (HEADS 43.44)

ENTER A "8" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:   8  COPY FROM:   8  ACTIVE:  M   FALSE
IF     VEH YELLOW ON PH      5     IS  ON

THEN   SIG SET OLP YELLOW    3        ON


ELSE
```

LOGIC FOR YELLOW ARROW CLEARANCE WHEN LEAVING PHASE 5 (HEADS 43.44)

ENTER A "9" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:   9  COPY FROM:   9  ACTIVE:  M   FALSE
IF     CTR PHASE TIMING      5     IS  ON
AND    VEH RED ON PHASE      5     IS  ON

THEN   SIG SET OLP RED       3        ON


ELSE
```

LOGIC FOR RED SIGNAL CLEARANCE WHEN LEAVING PHASE 5 (HEADS 43.44)

ENTER A "10" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:  10  COPY FROM:  10  ACTIVE:  M   FALSE
IF     VEH OVERLAP           8     IS  ON

THEN   SIG SET OVLP GREEN    4        OFF


ELSE
```

LOGIC FOR TURNING FLASHING YELLOW ARROW OFF DURING OLH. WHICH HAS PARENT PHASE 3 (HEADS 24.25)

ENTER A "11" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:  11  COPY FROM:  11  ACTIVE:  M   FALSE
IF     VEH OVERLAP YLW       8     IS  ON

THEN   SIG SET OLP YELLOW    4        ON


ELSE
```

LOGIC FOR YELLOW ARROW CLEARANCE WHEN LEAVING OLH. WHICH HAS PARENT PHASE 3 (HEADS 24.25)

ENTER A "12" IN THE LP# FIELD. PRESS 'ENTER'. AND PROGRAM AS SHOWN.

```
LP#:  12  COPY FROM:  12  ACTIVE:  M   FALSE
IF     VEH OVERLAP           8     IS  ON
AND    VEH OVERLAP RED       8     IS  ON

THEN   SIG SET OLP RED       4        ON


ELSE
```

LOGIC FOR RED SIGNAL CLEARANCE WHEN LEAVING OLH. WHICH HAS PARENT PHASE 3 (HEADS 24.25)

END PROGRAMMING

4. From the LOGIC PROCESSOR Submenu select **1. LOGIC STATEMENT CONTROL**

ENABLE LOGIC PROCESSOR STATEMENTS 1-3 BY POSITIONING THE CURSOR OVER THE FIELDS SHOWN BELOW AND USING THE TOGGLE KEY TO ENABLE THEM.

```
LOGIC STATEMENT CONTROL
          1  2  3  4  5  6  7  8  9  0  1  2  3  4  5  6
LP 1-15   E  E  E  E  E  E  E  E  E  E  E  E  .  .  .  .
LP 16-30  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
LP 31-45  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
LP 46-60  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
LP 61-75  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
LP 76-90  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
```

END PROGRAMMING

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 06-0155
DESIGNED: January 2016
SEALED: 8/29/2016
REVISED: N/A

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED

ELECTRICAL AND PROGRAMMING DETAILS FOR:

US 401 Bus (Raeford Road)
at
NC 59 (Hope Mills Road)/
SR 1596 (Glensford Drive)

Division 6 | Cumberland County | Fayetteville

PLAN DATE:	June 2016	REVIEWED BY:	BAS
PREPARED BY:	S. Armstrong	REVIEWED BY:	

REVISIONS	INIT.	DATE

Prepared in the Offices of:
Transportation Mobility and Safety Division
NC DEPARTMENT OF TRANSPORTATION
Signals Management Section
750 N.Greenfield Pkwy,Garner,NC 27529

SEAL
NORTH CAROLINA PROFESSIONAL SEAL 036880 ENGINEER KEITH M. MIMS

DocuSigned by: Keith M. Mims 10/13/2016
2F8078BE8CD34A5... DATE

SIG. INVENTORY NO. 06-0155