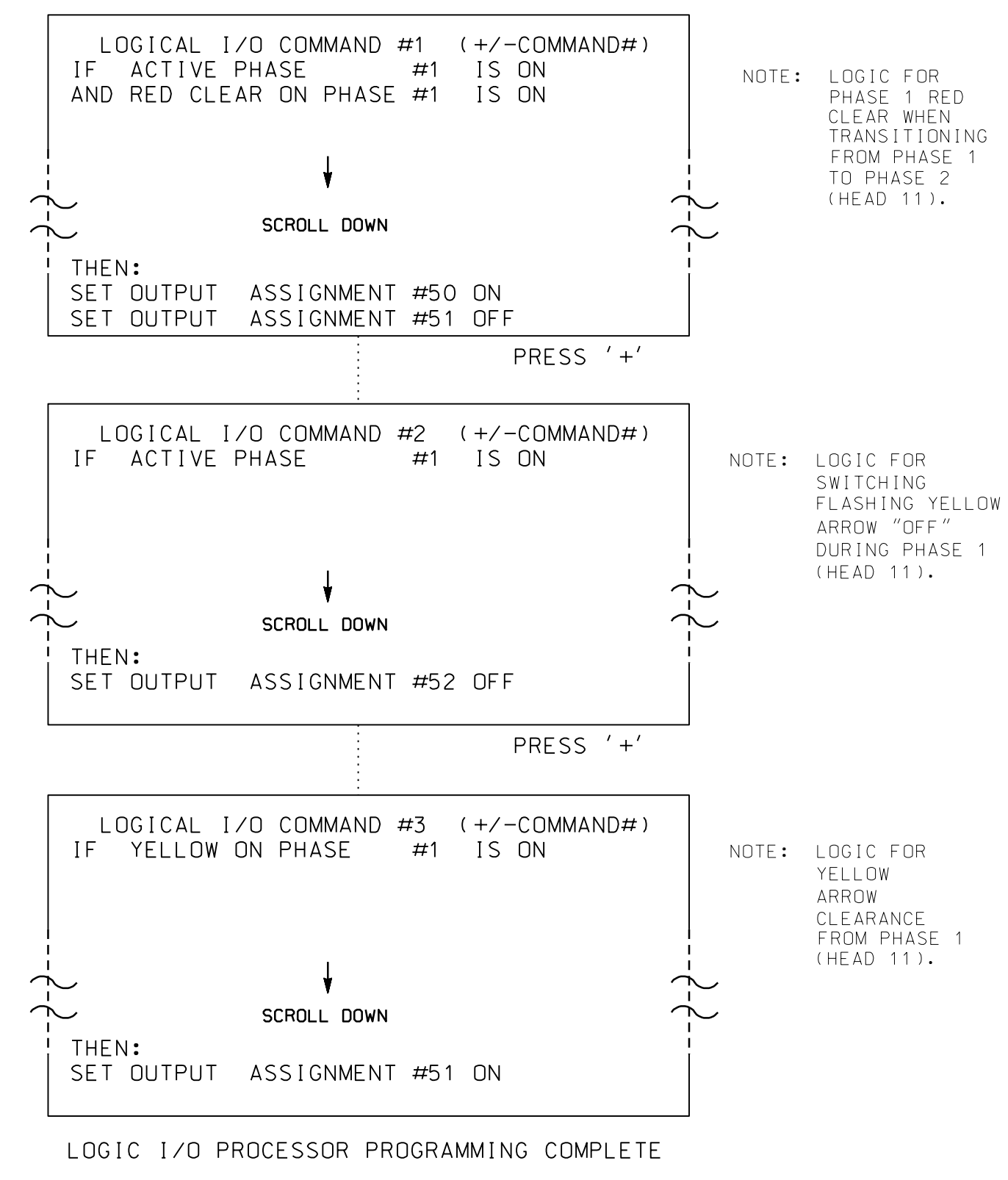


### LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2 AND 3.
- FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



OUTPUT REFERENCE SCHEDULE	
USE TO INTERPRET LOGIC PROCESSOR	
OUTPUT 50	= Overlap A Red
OUTPUT 51	= Overlap A Yellow
OUTPUT 52	= Overlap A Green

### OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

```

PAGE 1: VEHICLE OVERLAP 'A' SETTINGS
PHASE:          ;12345678910111213141516
VEH OVL PARENTS: ;XX
VEH OVL NOT VEH: ;
VEH OVL NOT PED: ;
VEH OVL GRN EXT: ;
STARTUP COLOR:  - RED  - YELLOW  - GREEN
FLASH COLORS:   - RED  - YELLOW  X GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0-255 SEC).....0
YELLOW CLEAR (0=PARENT,3-25.5 SEC)..0.0
RED CLEAR (0=PARENT,0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)....0
    
```

← NOTICE GREEN FLASH

PRESS '+' TWICE

```

PAGE 1: VEHICLE OVERLAP 'C' SETTINGS
PHASE:          ;12345678910111213141516
VEH OVL PARENTS: ; X
VEH OVL NOT VEH: ;
VEH OVL NOT PED: ;
VEH OVL GRN EXT: ;
STARTUP COLOR:  - RED  - YELLOW  - GREEN
FLASH COLORS:   - RED  - YELLOW  X GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0-255 SEC).....0
YELLOW CLEAR (0=PARENT,3-25.5 SEC)..0.0
RED CLEAR (0=PARENT,0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)....0
    
```

← NOTICE GREEN FLASH

OVERLAP PROGRAMMING COMPLETE

### COUNTDOWN PEDESTRIAN SIGNAL OPERATION

Countdown Ped Signals are required to display timing only during Ped Clearance Interval. Consult Ped Signal Module user's manual for instructions on selecting this feature.

### BACKUP PROTECTION NOTE

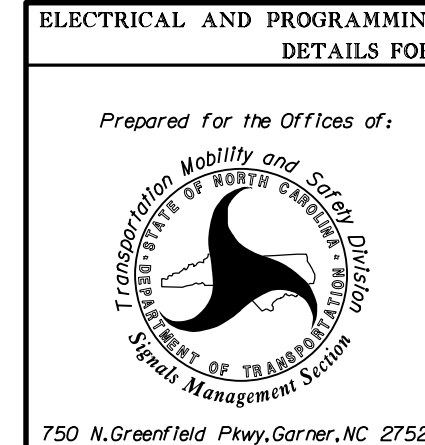
(program controller as shown below)

From Main Menu press '2' (Phase Control), then '1' (Phase Control Functions). Deselect phase 6 for 'Backup Protect'.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 10-2010  
DESIGNED: March 2016  
SEALED: July 7, 2016  
REVISED:

Signal Upgrade - Final Design  
Electrical Detail Sheet 2 of 2

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



SR 1445 (Derita Road) at Thunder Road / PNG Driveway	
Division 10	Cabarrus County
PLAN DATE: March 2016	REVIEWED BY: J O Deaton
PREPARED BY: M W Yalch	REVIEWED BY:
REVISIONS	INIT. DATE

DocuSigned by:  
**James O. Deaton**  
7/11/2016  
40FFBAC30B06F

7/11/2016 10:40:02 AM C:\Users\jwalch\Documents\CAD\10-2010\10-2010-03-166.dgn