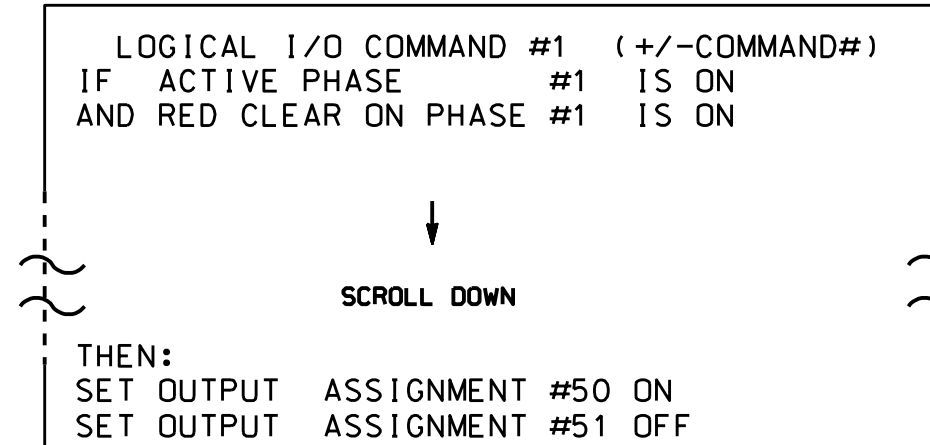
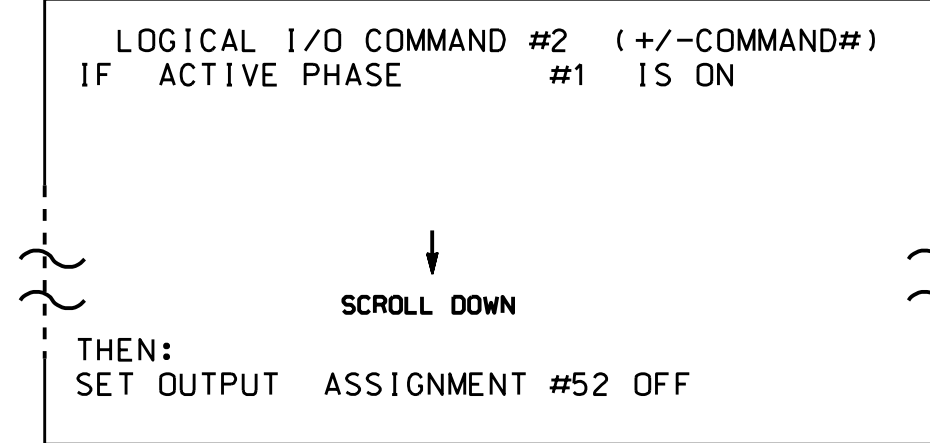


LOGICAL I/O PROCESSOR PROGRAMMING DETAIL
TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE
(program controller as shown below)

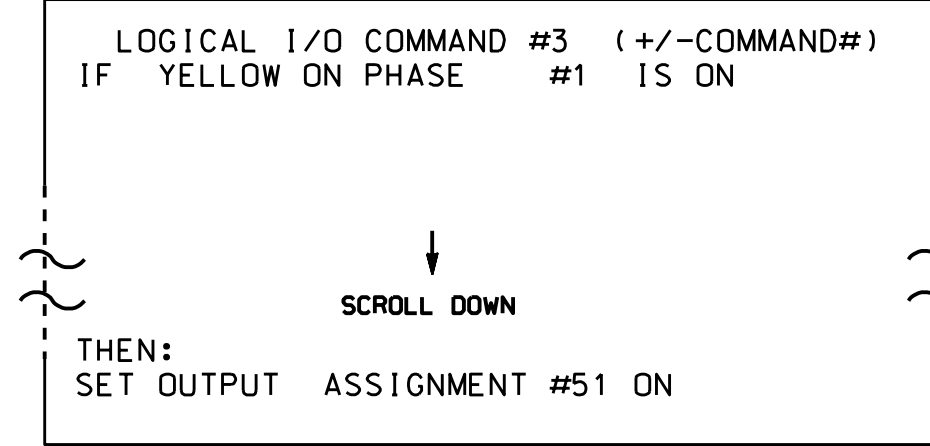
- FROM MAIN MENU PRESS '2' (PHASE CONTROL). THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12 AND 13.
- FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



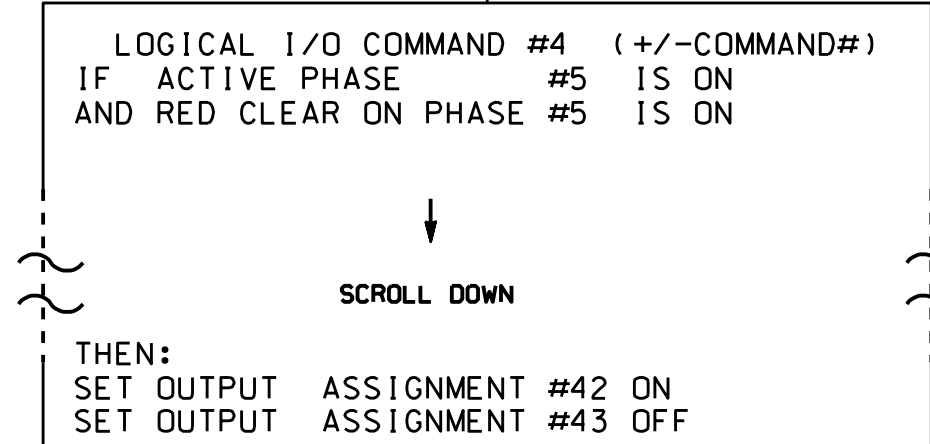
NOTE: LOGIC FOR PHASE 1 RED CLEAR WHEN TRANSITIONING FROM PHASE 1 TO PHASE 2 (HEAD 11).



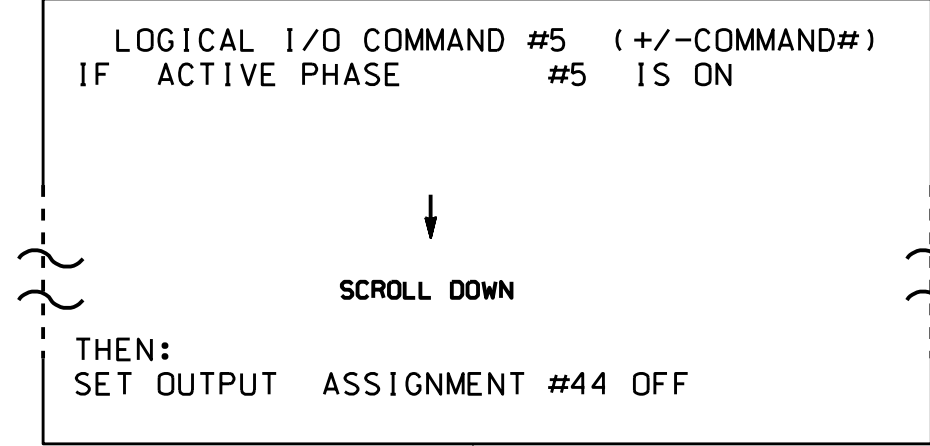
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 1 (HEAD 11).



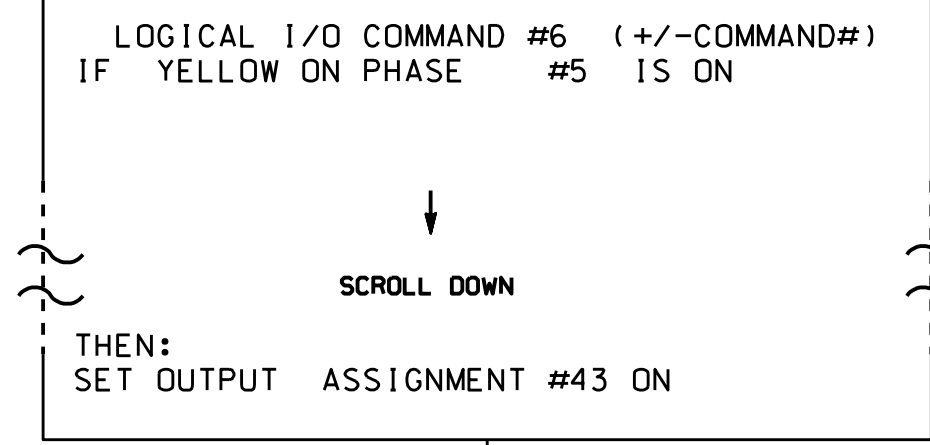
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 1 (HEAD 11).



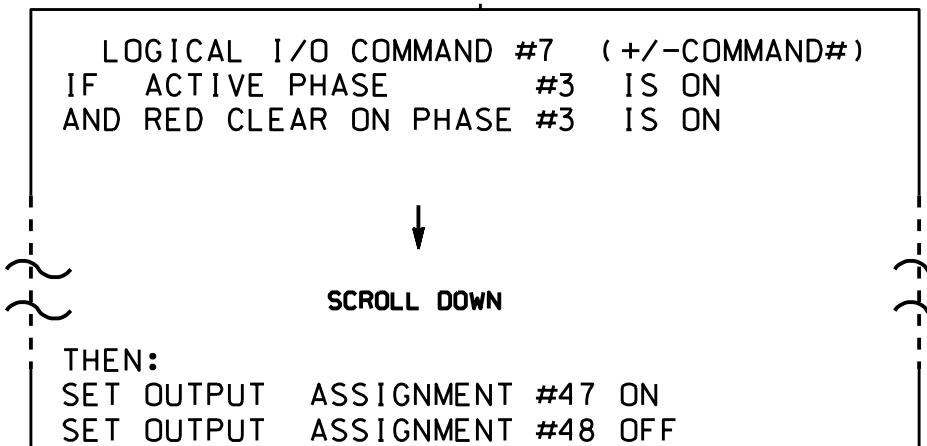
NOTE: LOGIC FOR PHASE 5 RED CLEAR WHEN TRANSITIONING FROM PHASE 5 TO PHASE 6 (HEAD 51).



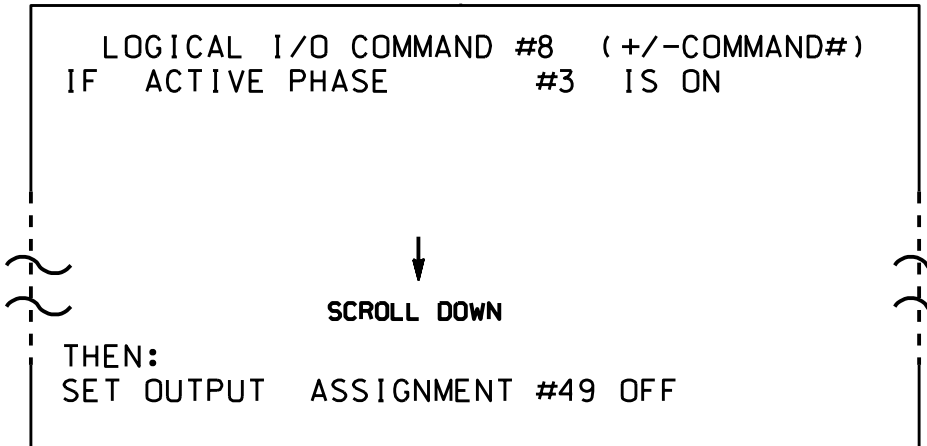
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 5 (HEAD 51).



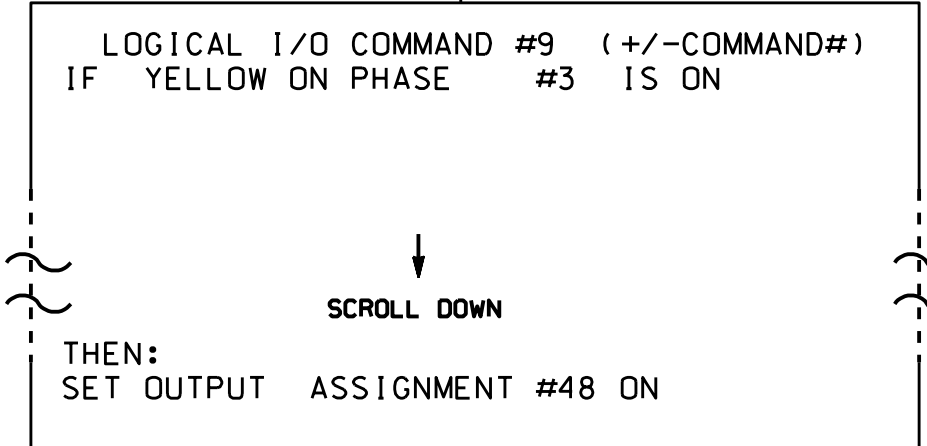
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 5 (HEAD 51).



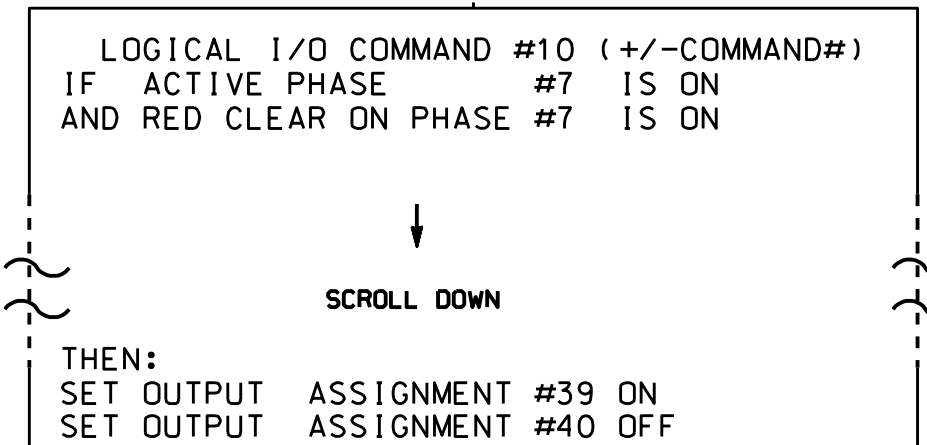
NOTE: LOGIC FOR PHASE 3 RED CLEAR WHEN TRANSITIONING FROM PHASE 3 TO PHASE 4 (HEAD 31).



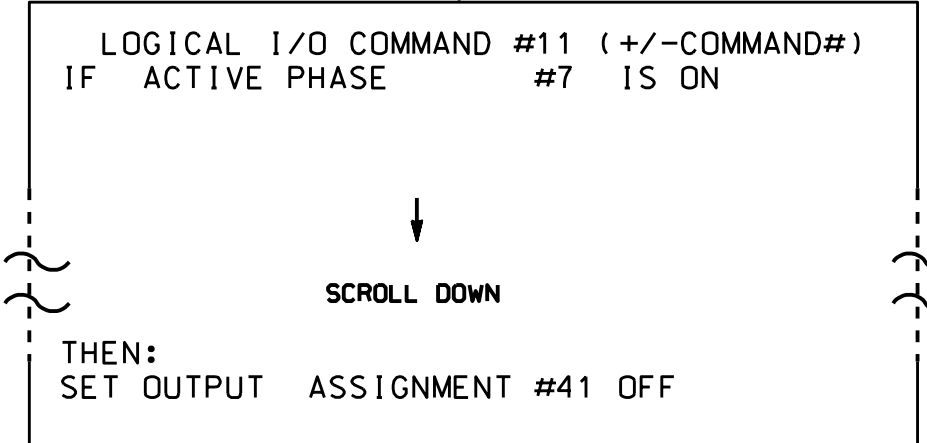
NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 3 (HEAD 31).



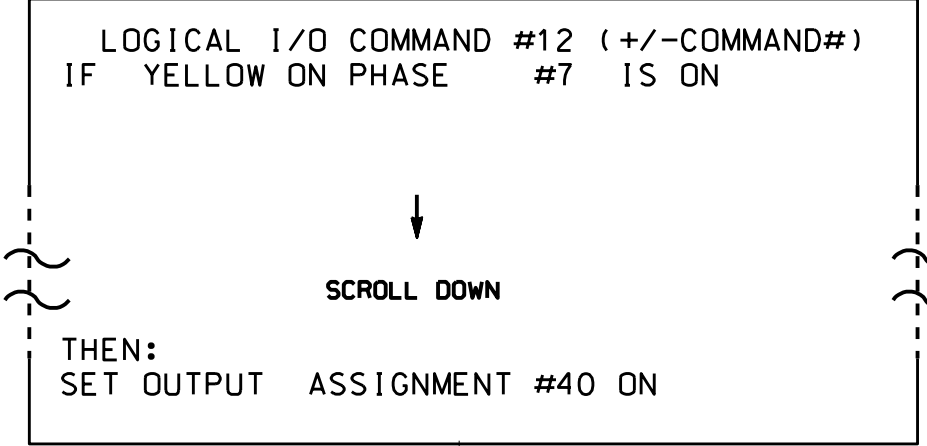
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 3 (HEAD 31).



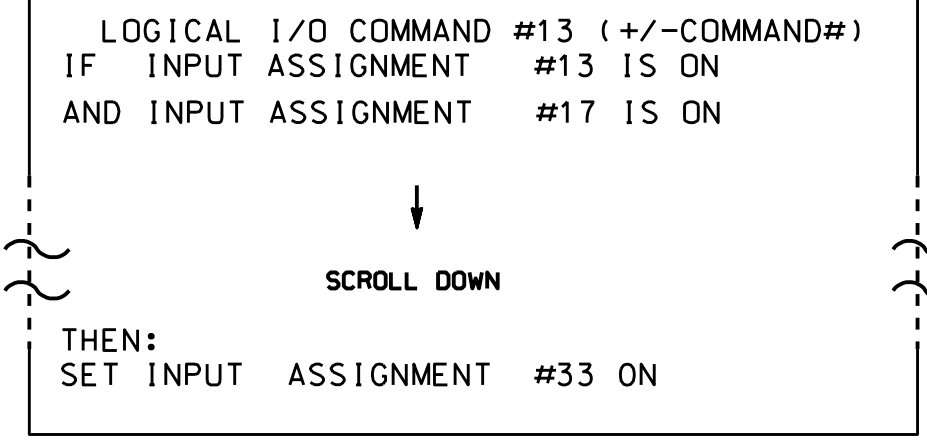
NOTE: LOGIC FOR PHASE 7 RED CLEAR WHEN TRANSITIONING FROM PHASE 7 TO PHASE 8 (HEAD 71).



NOTE: LOGIC FOR SWITCHING FLASHING YELLOW ARROW "OFF" DURING PHASE 7 (HEAD 71).



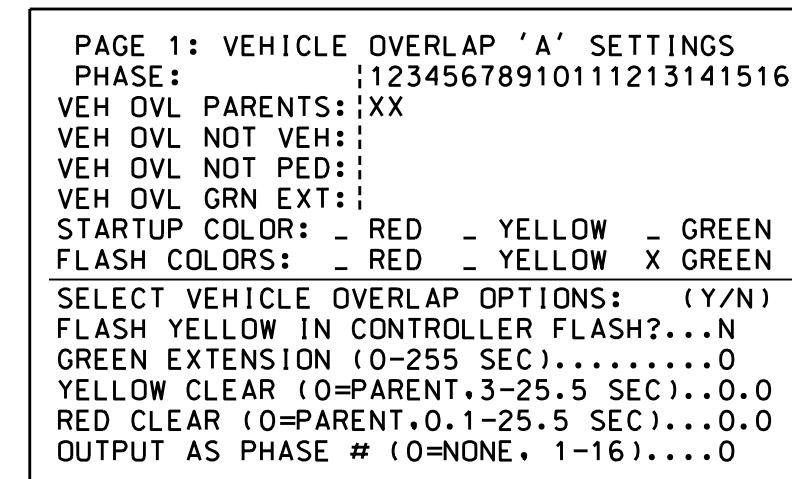
NOTE: LOGIC FOR YELLOW ARROW CLEARANCE FROM PHASE 7 (HEAD 71).



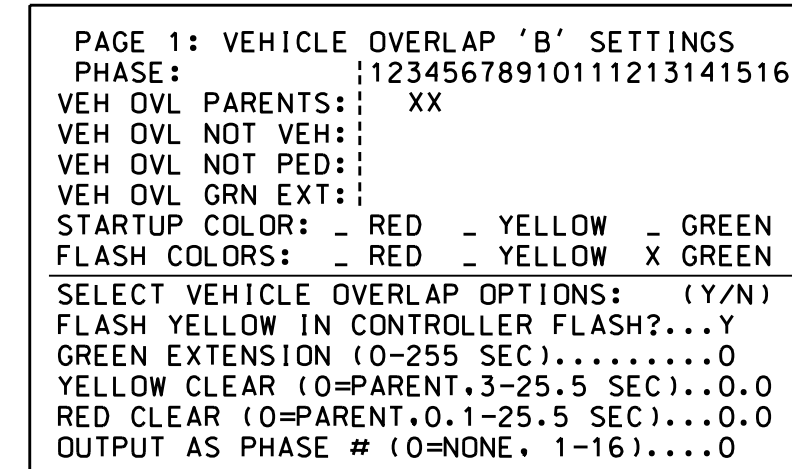
LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OVERLAP PROGRAMMING DETAIL
(program controller as shown below)

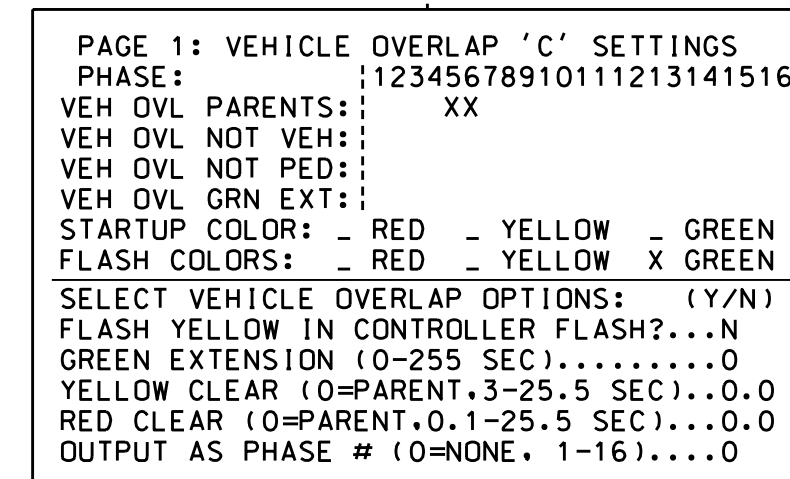
FROM MAIN MENU PRESS '8' (OVERLAPS). THEN '1' (VEHICLE OVERLAP SETTINGS).



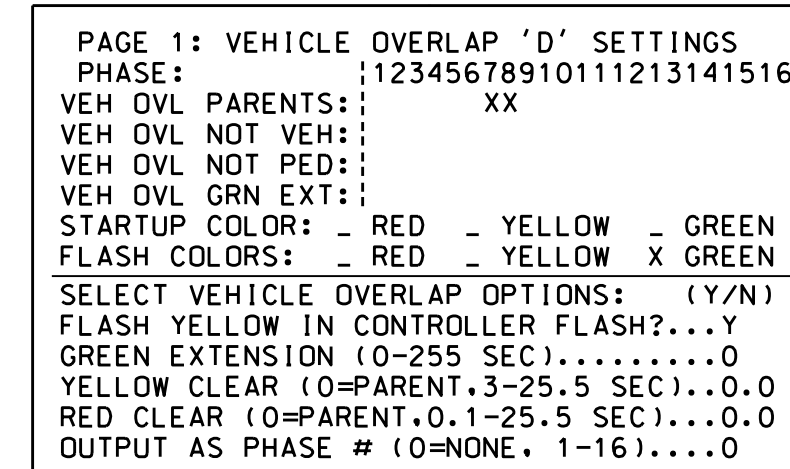
NOTICE GREEN FLASH



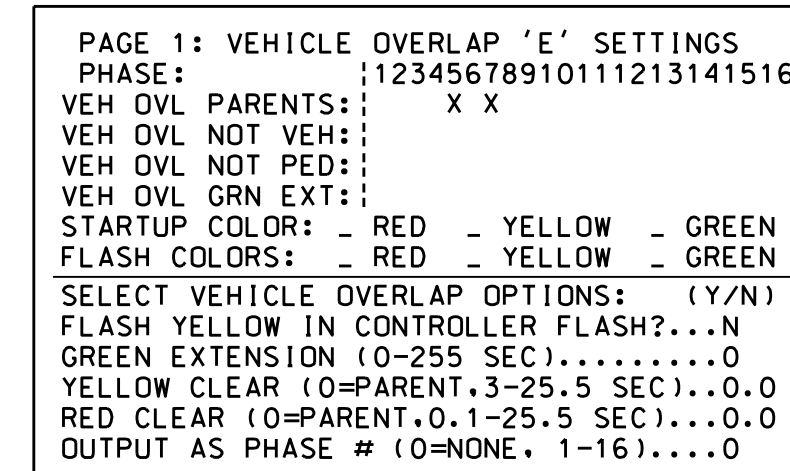
NOTICE GREEN FLASH



NOTICE GREEN FLASH



NOTICE GREEN FLASH



OVERLAP PROGRAMMING COMPLETE

FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

- ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
- ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
- REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

OUTPUT REFERENCE SCHEDULE
 USE TO INTERPRET LOGIC PROCESSOR

OUTPUT 39	=	Overlap D Red
OUTPUT 40	=	Overlap D Yellow
OUTPUT 41	=	Overlap D Green
OUTPUT 42	=	Overlap C Red
OUTPUT 43	=	Overlap C Yellow
OUTPUT 44	=	Overlap C Green
OUTPUT 47	=	Overlap B Red
OUTPUT 48	=	Overlap B Yellow
OUTPUT 49	=	Overlap B Green
OUTPUT 50	=	Overlap A Red
OUTPUT 51	=	Overlap A Yellow
OUTPUT 52	=	Overlap A Green
INPUT 13	=	PREEMPT 1 INPUT
INPUT 14	=	PREEMPT 2 INPUT
INPUT 33	=	PREEMPT 3 INPUT

THIS ELECTRICAL DETAIL IS FOR
 THE SIGNAL DESIGN: 08-0707
 DESIGNED: July 2014
 SEALED: 5-06-15
 REVISED: N/A

ELECTRICAL DETAIL SHEET 2 OF 5

	SR 1595 (Surrett Drive) at SR 1592 (Eden Terrace) and Corporation Drive	SEAL JOHN T. ROWE, JR. ENGINEER 008453
	Prepared In the Offices of: 	Division 8 Randolph County Archdale PLAN DATE: July 2014 REVIEWED BY: JTR PREPARED BY: James Peterson REVIEWED BY:
750 N. Greenfield Pkwy, Garner, NC 27529	REVISIONS INIT. DATE	SIG. INVENTORY NO. 08-0707