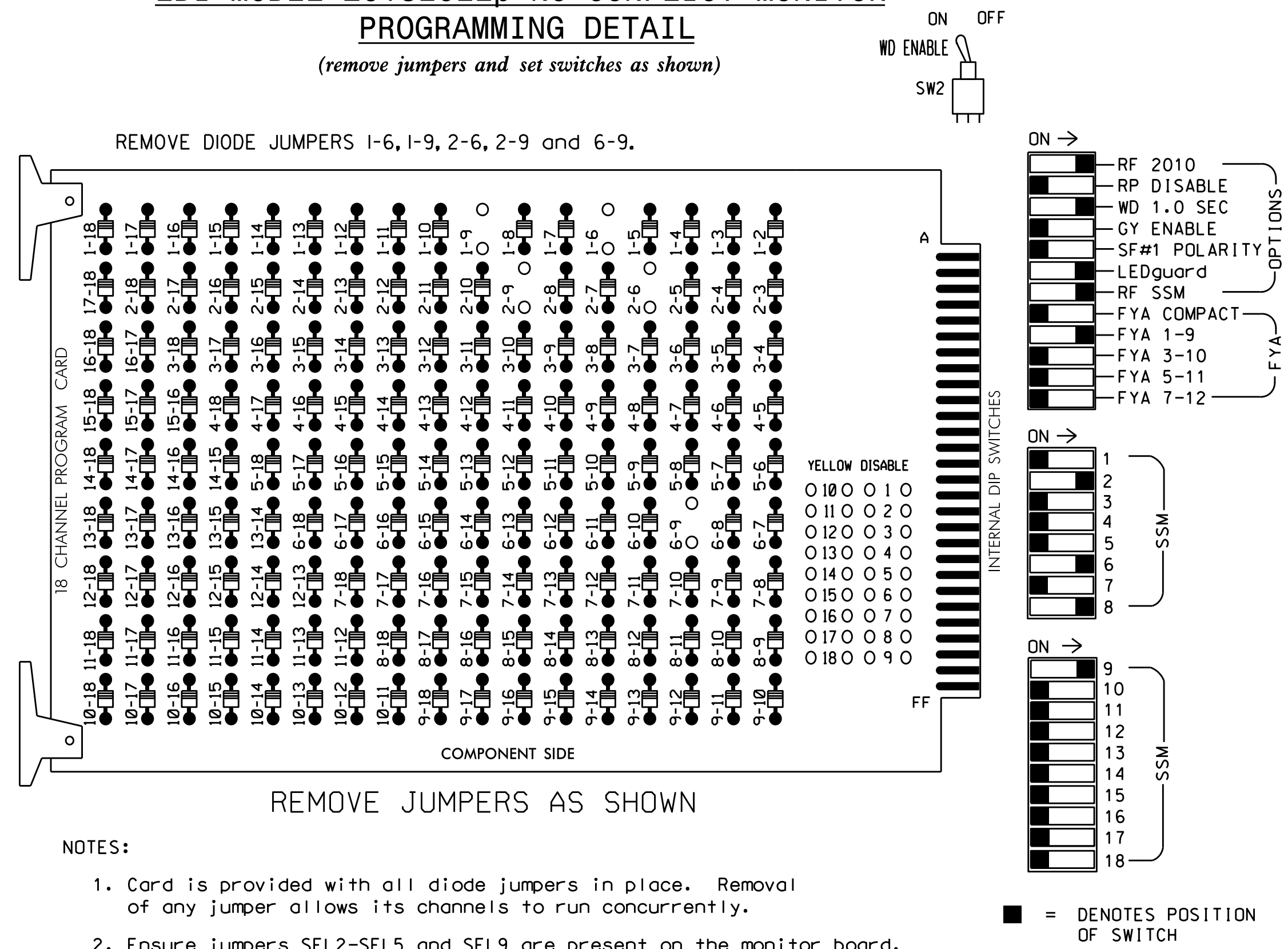


EDI MODEL 2018ECLip-NC CONFLICT MONITOR
PROGRAMMING DETAIL

(remove jumpers and set switches as shown)



NOTES:

1. Card is provided with all diode jumpers in place. Removal of any jumper allows its channels to run concurrently.
2. Ensure jumpers SEL2-SEL5 and SEL9 are present on the monitor board.
3. Ensure that Red Enable is active at all times during normal operation.
4. Integrate monitor with Ethernet network in cabinet.

NOTES

1. To prevent "flash-conflict" problems, insert red flash program blocks for all unused vehicle load switches in the output file. The installer shall verify that signal heads flash in accordance with the Signal Plans.
2. Enable Simultaneous Gap-Out for all phases.
3. Program phases 2 and 6 for Variable Initial and Gap Reduction.
4. Program phases 2 and 6 for Start Up In Green.
5. Program phases 2 and 6 for Yellow Flash, and overlap 1 as Wag Overlaps.
6. The cabinet and controller are part of the High Point Signal System.

EQUIPMENT INFORMATION

CONTROLLER.....2070L
 CABINET.....332 /W/ AUX
 SOFTWARE.....ECONOLITE OASIS
 CABINET MOUNT.....BASE
 OUTPUT FILE POSITIONS...18 WITH AUX. OUTPUT FILE
 LOAD SWITCHES USED.....S1,S2,S8,S11,AUX S1.
 PHASES USED.....1,2,6,8.
 OVERLAP "A".....1+2
 OVERLAP "B".....NOT USED
 OVERLAP "C".....NOT USED
 OVERLAP "D".....NOT USED

SIGNAL HEAD HOOK-UP CHART

LOAD SWITCH NO.	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	AUX S1	AUX S2	AUX S3	AUX S4	AUX S5	AUX S6	
CMU CHANNEL NO.	1	2	13	3	4	14	5	6	15	7	8	16	9	10	17	11	12	18	
PHASE	1	2	2 PED	3	4	4 PED	5	6	6 PED	7	8	8 PED	OLA	OLB	SPARE	OLC	OLD	SPARE	
SIGNAL HEAD NO.	11	21,22	NU	NU	NU	NU	NU	61,62	NU	NU	81,82	NU	11	NU	NU	NU	NU	NU	
RED		128						134			107								
YELLOW	*	129						135			108								
GREEN		130						136			109								
RED ARROW																		A121	
YELLOW ARROW																			A122
FLASHING YELLOW ARROW																			A123
GREEN ARROW	127																		

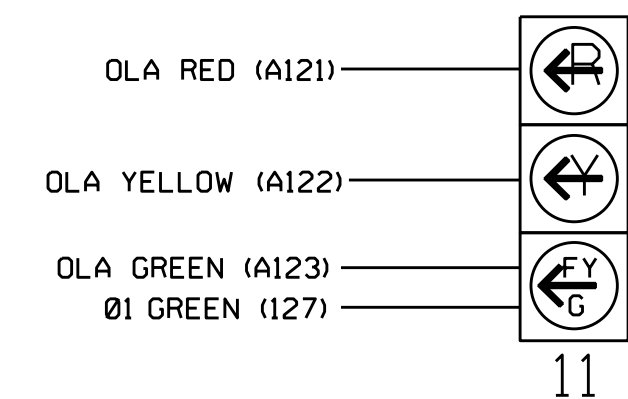
NU = Not Used

* Denotes install load resistor. See load resistor installation detail this sheet.

* See pictorial of head wiring in detail below.

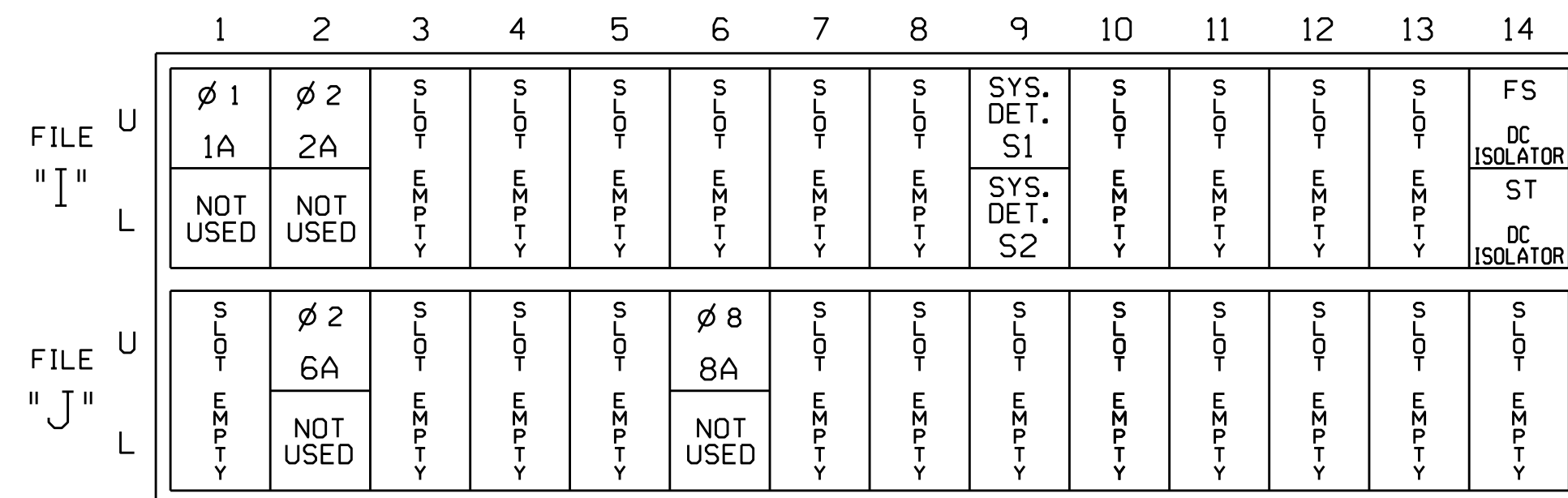
BIMODAL SECTION FYA SIGNAL WIRING DETAIL

(wire signal heads as shown)



INPUT FILE POSITION LAYOUT

(front view)



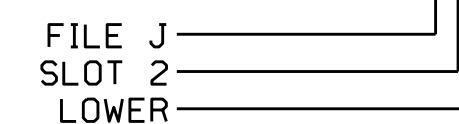
EX.: 1A, 2A, ETC. = LOOP NO.'S

FS = FLASH SENSE
 ST = STOP TIME

INPUT FILE CONNECTION & PROGRAMMING CHART

LOOP NO.	LOOP TERMINAL	INPUT FILE POS.	PIN NO.	INPUT ASSIGNMENT NO.	DETECTOR NO.	NEMA PHASE	CALL	EXTEND	FULL TIME DELAY	STRETCH TIME	DELAY TIME
1A	TB2-1,2	I1U	56	18	1	1	Y	Y			15
2A	TB2-5,6	I2U	39	1	2	2	Y	Y			
6A	TB3-5,6	J2U	40	2	6	6	Y	Y			
8A	TB5-9,10	J6U	42	4	8	8	Y	Y			10
* S1	TB6-9,10	I9U	60	22	11	SYS					
* S2	TB6-11,12	I9L	62	24	13	SYS					

INPUT FILE POSITION LEGEND: J2L



NOTE

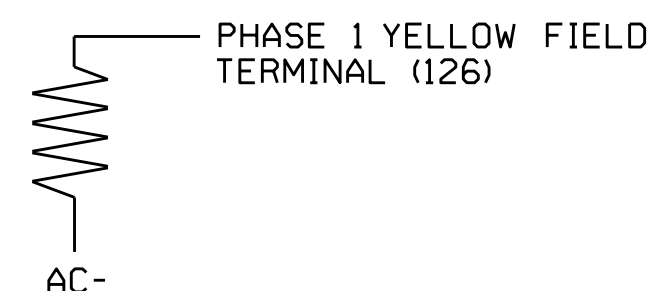
1. The sequence display for this signal requires special logic programming. See sheet 2 for programming instructions.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 07-1461
 DESIGNED: April 2014
 SEALED: 3-31-15
 REVISED: N/A

LOAD RESISTOR INSTALLATION DETAIL

(install resistors as shown below)

ACCEPTABLE VALUES	
VALUE (ohms)	WATTAGE
1.5K - 1.9K	25W (min)
2.0K - 3.0K	10W (min)



ELECTRICAL DETAIL SHEET 1 OF 2

ELECTRICAL AND PROGRAMMING DETAILS FOR: Prepared in the Offices of: 750 N. Greenfield Pkwy, Garner, NC 27529	SR 1486 (W. Main Street) at SR 1332 (Scientific Street)		SEAL JOHN T. ROWE, JR. ENGINEER
	Division 7 Guilford County, NC PLAN DATE: August 2014 PREPARED BY: James Peterson	JTB REVIEWED BY: REVISIONS INIT. DATE	

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