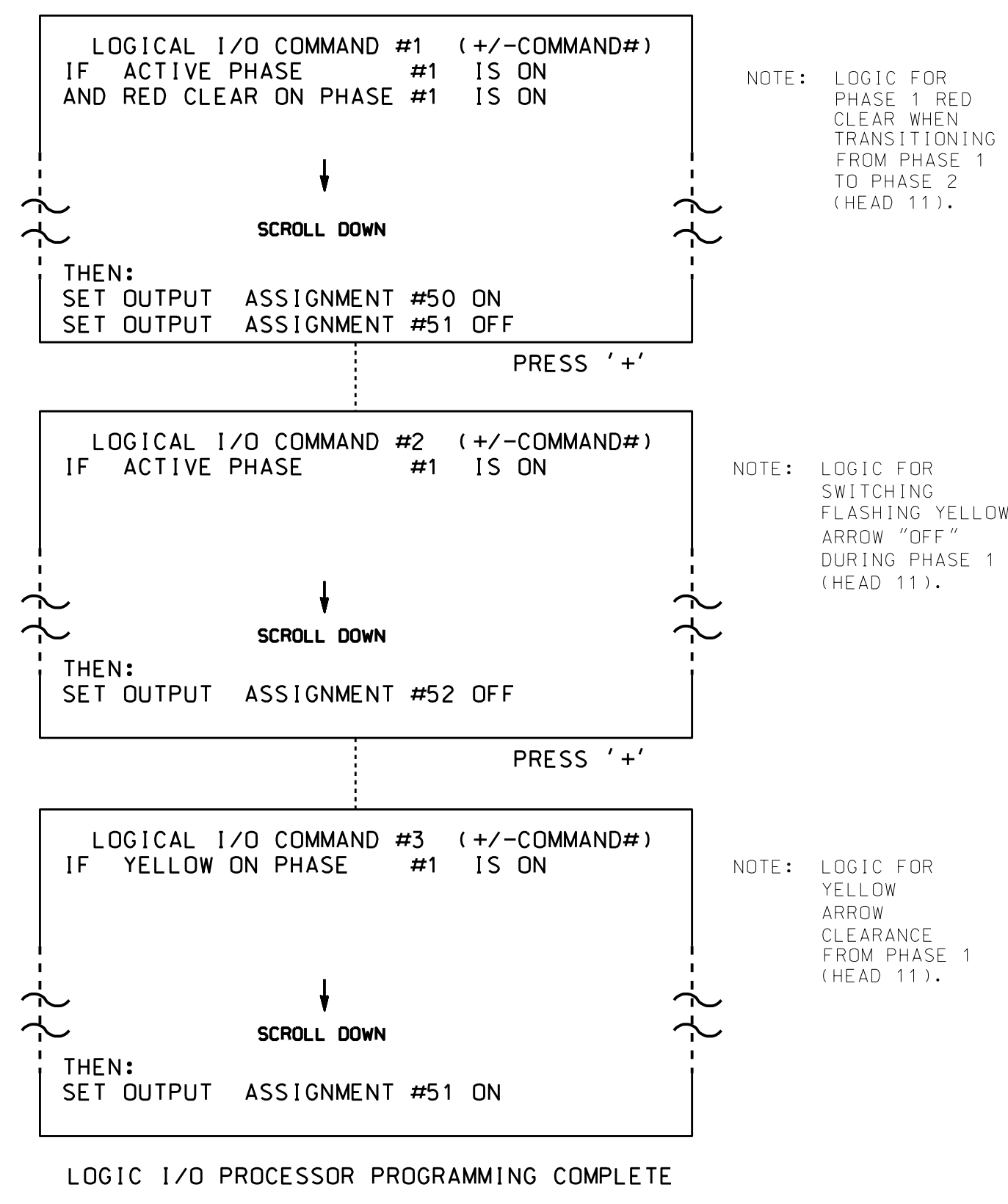


LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



OUTPUT REFERENCE SCHEDULE

OUTPUT 50 = Overlap A Red
OUTPUT 51 = Overlap A Yellow
OUTPUT 52 = Overlap A Green

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

```

PAGE 1: VEHICLE OVERLAP 'A' SETTINGS
PHASE:      12345678910111213141516
VEH OVL PARENTS: XX
VEH OVL NOT VEH:
VEH OVL NOT PED:
VEH OVL GRN EXT:
STARTUP COLOR:  _ RED  _ YELLOW  _ GREEN
FLASH COLORS:  _ RED  _ YELLOW  X GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0-255 SEC)...0.0
YELLOW CLEAR (0=PARENT,3-25.5 SEC)..0.0
RED CLEAR (0=PARENT,0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0
    
```

← NOTICE GREEN FLASH

PRESS '+\' TWICE

```

PAGE 1: VEHICLE OVERLAP 'C' SETTINGS
PHASE:      12345678910111213141516
VEH OVL PARENTS: X
VEH OVL NOT VEH:
VEH OVL NOT PED:
VEH OVL GRN EXT:
STARTUP COLOR:  _ RED  _ YELLOW  _ GREEN
FLASH COLORS:  _ RED  _ YELLOW  X GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0-255 SEC)...0.0
YELLOW CLEAR (0=PARENT,3-25.5 SEC)..0.0
RED CLEAR (0=PARENT,0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0
    
```

← NOTICE GREEN FLASH

PRESS '+/-' TO ADVANCE TO OVERLAP 'P'

```

PAGE 1: VEHICLE OVERLAP 'P' SETTINGS
PHASE:      12345678910111213141516
VEH OVL PARENTS: XX X X X
VEH OVL NOT VEH:
VEH OVL NOT PED:
VEH OVL GRN EXT:
STARTUP COLOR:  _ RED  _ YELLOW  _ GREEN
FLASH COLORS:  _ RED  _ YELLOW  _ GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...N
GREEN EXTENSION (0-255 SEC)...0.0
YELLOW CLEAR (0=PARENT,3-25.5 SEC)..0.0
RED CLEAR (0=PARENT,0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0
    
```

OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 07-1268
DESIGNED: August 2014
SEALED: 4/21/2015
REVISED: N/A

Electrical Detail - Sheet 2 of 5

<p>Prepared In the Offices of:</p> <p>750 N. Greenfield Pkwy, Garner, NC 27529</p>	<p>SR 1486 (W. Main Street) at SR 1334 (Dillon Rd.) and Ragsdale Rd.</p> <p>Division 7 Guilford County ds Jamestown</p> <p>PLAN DATE: January 2015 REVIEWED BY: <i>JTR</i></p> <p>PREPARED BY: S. Armstrong REVIEWED BY:</p>	<p>SEAL</p> <p>DocuSigned by: <i>John T. Rowe, Jr.</i> 4/22/2015</p> <p>SIG. INVENTORY NO. 07-1268</p>									
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 80%;">REVISIONS</th> <th style="width: 10%;">INIT.</th> <th style="width: 10%;">DATE</th> </tr> </thead> <tbody> <tr> <td> </td> <td> </td> <td> </td> </tr> <tr> <td> </td> <td> </td> <td> </td> </tr> </tbody> </table>			REVISIONS	INIT.	DATE						
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 sarmstrong