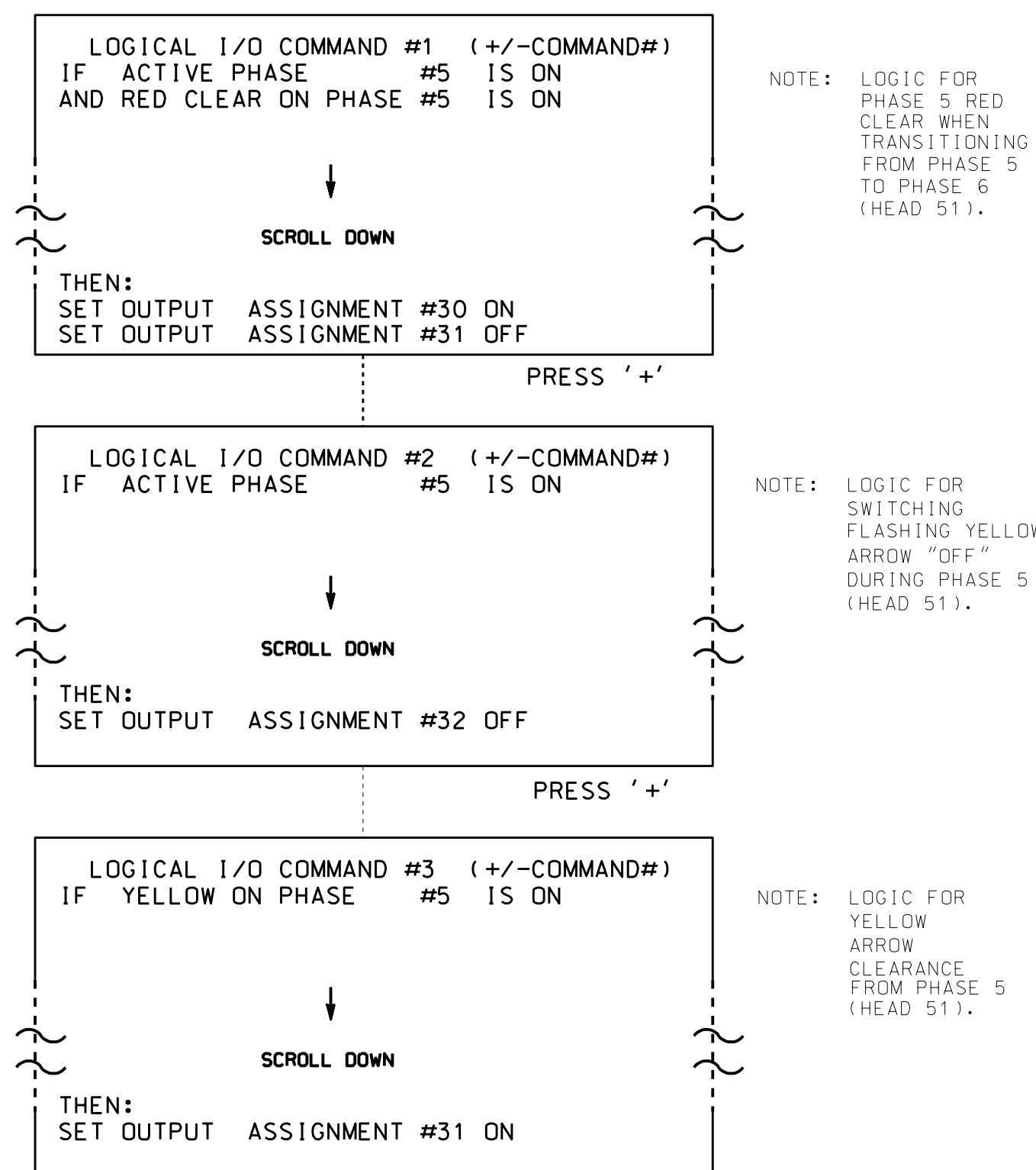


LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS), SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
- FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

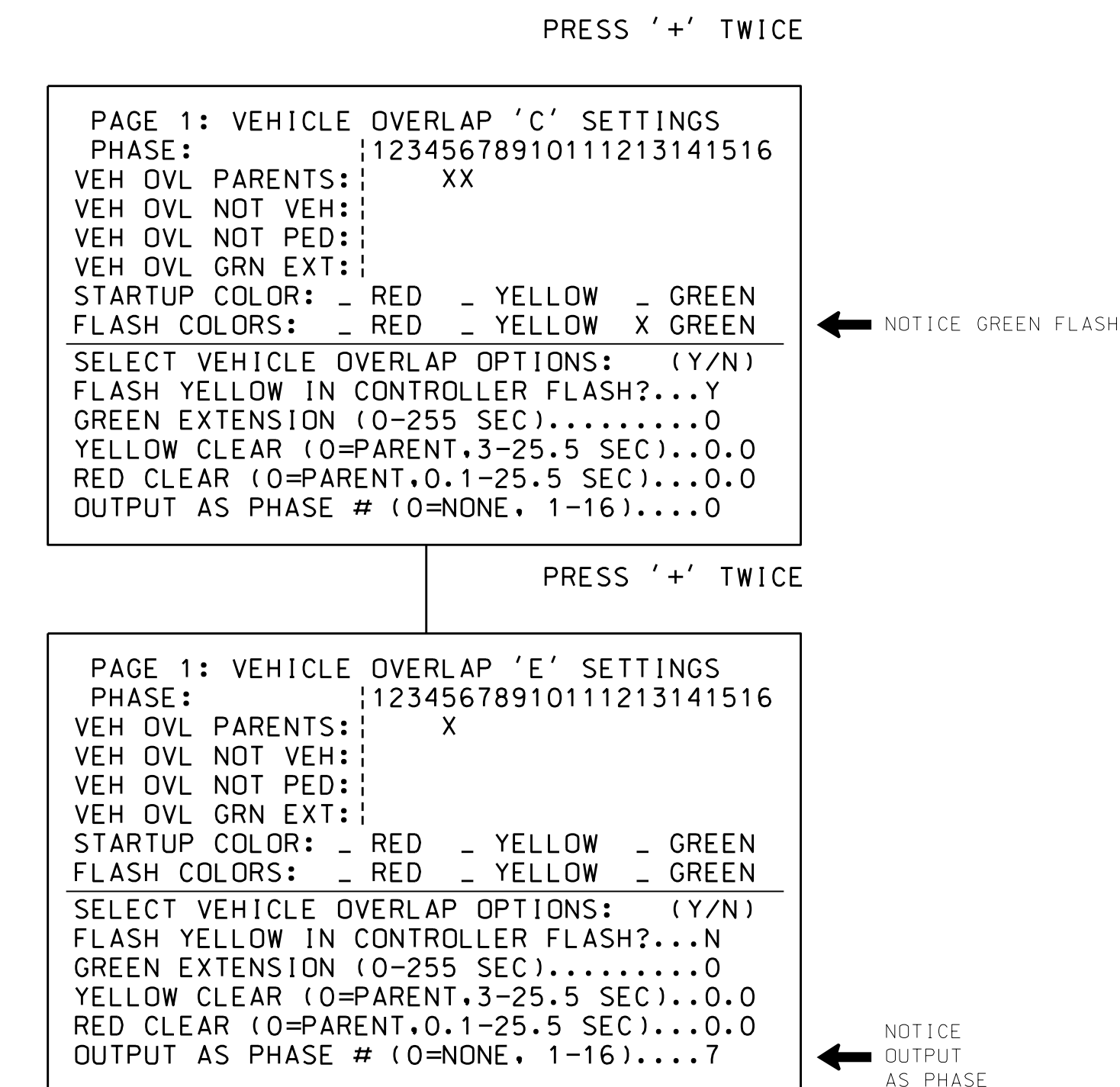
OUTPUT REFERENCE SCHEDULE
OUTPUT 30 = Overlap C Red
OUTPUT 31 = Overlap C Yellow
OUTPUT 32 = Overlap C Green
OUTPUT 34 = Phase 5 Green

Note: All outputs shown above have been remapped. See sheets 3 and 4 of this electrical detail.

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

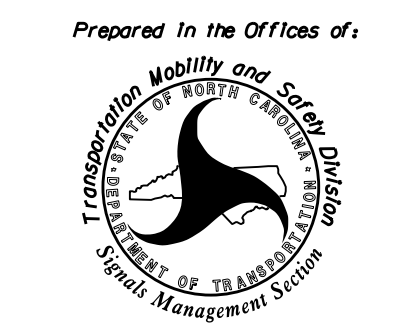
FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).



OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 11-1174 T3
DESIGNED: May 2015
SEALED: 5/22/2015
REVISED: N/A

Electrical Detail - Temporary Signal 3 (TCP Phase III) - Sheet 3 of 3

ELECTRICAL AND PROGRAMMING DETAILS FOR:	US 421 at US 221	SEAL NORTH CAROLINA PROFESSIONAL ENGINEER SEAL 008453 JOHN T. ROWE, JR.
Prepared In the Offices of:  750 N. Greenfield Pkwy, Garner, NC 27529	Division 11 Watauga County DE Deep Gap PLAN DATE: May 2015 REVIEWED BY: JTR PREPARED BY: S. Armstrong REVIEWED BY:	DocuSigned by: John T. Rowe, Jr. 5/26/2015 041183GNMETSMB DATE
	REVISIONS INIT. DATE	SIG. INVENTORY NO. 11-1174 T3

05-MAY-2015 07:01
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