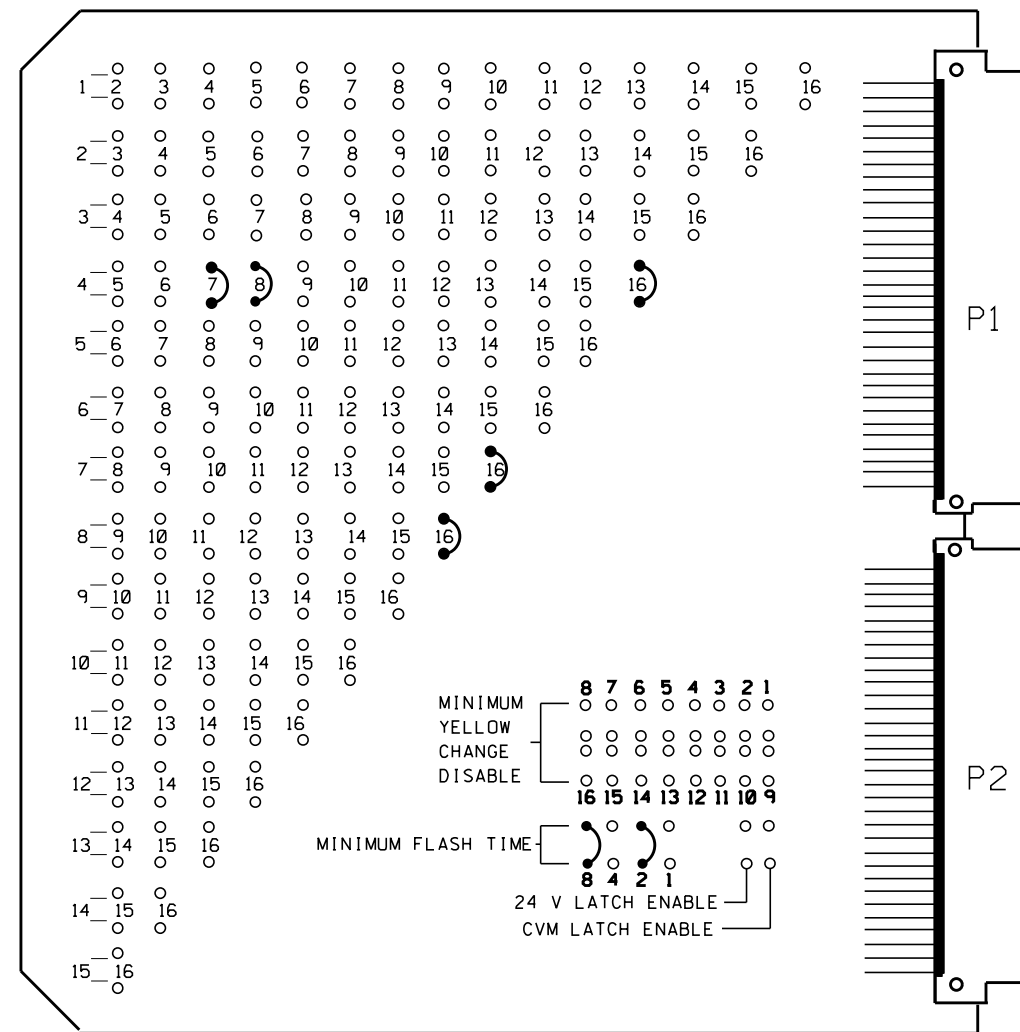


**EDI MODEL MMU2-16LE
MALFUNCTION MANAGEMENT UNIT
PROGRAMMING DETAIL**
(program card and tables as shown below)



MMU PROGRAMMING CARD

CHANNEL NUMBER	ENABLE/DISABLE
1	DISABLE
2	DISABLE
3	DISABLE
4	ENABLE
5	DISABLE
6	ENABLE
7	ENABLE
8	ENABLE
9	DISABLE
10	DISABLE
11	DISABLE
12	DISABLE
13	DISABLE
14	DISABLE
15	DISABLE
16	ENABLE

MMU PROGRAMMING NOTE
ENSURE YELLOW CHANGE PLUS RED CLEARANCE MONITORING IS ENABLED FOR ALL CHANNELS.

OPTION	SETTING
RECURRENT PULSE	ON
WALK DISABLE	OFF
LOG CVM FAILTS	ON
EXTERN WATCHDOG	OFF
24V-2-12VDC	OFF
PGM CARD MEMORY	ON
LEDguard	ON
FORCE TYPE 16	OFF
TYPE12-SDLC	OFF
VM 3x/Day Latch	ON

FLASHING YELLOW ARROW	
CONFIG MODE	A
ENABLE CHANNEL PAIR, FYA	
CH 1-9	OFF
CH 3-10	OFF
CH 5-11	OFF
CH 7-12	ON
RED/YEL INPUT ENABLE	
CH 1-9	OFF
CH 3-10	OFF
CH 5-11	OFF
CH 7-12	OFF
FLASH RATE FAULT	OFF
FYA TRAP DETECT	OFF

NOTES

- TO PREVENT "FLASH-CONFLICT" PROBLEMS, WIRE ALL UNUSED LOAD SWITCHES TO FLASH RED. VERIFY THAT SIGNAL HEADS FLASH IN ACCORDANCE WITH THE SIGNAL PLANS.
- TO PREVENT RED FAILURES ON UNUSED MONITOR CHANNELS, TIE UNUSED LOAD SWITCH RED OUTPUTS 1,2,3,5,9,10,11,12,13,14 &15 TO LOAD SWITCH AC+ BY INSERTING A JUMPER PLUG IN THE UNUSED LOAD SWITCH SOCKET FROM PIN 1 (LS AC+) TO PIN 3 (RED OUT). MAKE SURE ALL FLASH TRANSFER RELAYS ARE IN PLACE.
- PROGRAM CONTROLLER TO START UP IN PHASE 6 GREEN.
- SET POWER-UP FLASH TIME TO 10 SECONDS AND IMPLEMENT ON THE MALFUNCTION MANAGEMENT UNIT. SET CONTROLLER POWER-UP FLASH TIME TO 0 SECONDS.
- ENABLE SIMULTANEOUS GAP-OUT FEATURE, ON CONTROLLER UNIT, FOR ALL PHASES.
- PROGRAM DETECTORS IN ACCORDANCE WITH THE MANUFACTURER'S INSTRUCTIONS TO ACCOMPLISH THE DETECTION SCHEMES SHOWN ON THE SIGNAL DESIGN PLANS.
- PROGRAM DETECTOR CALL DELAY AND EXTENSION TIMING ON THE CONTROLLER, UNLESS OTHERWISE SPECIFIED.
- SET ALL DETECTOR CARD UNIT CHANNELS TO "PRESENCE" MODE.
- PROGRAM PHASES 4 AND 8, ON CONTROLLER UNIT, FOR DUAL ENTRY.
- THIS CONTROLLER AND CABINET ARE PART OF THE GREENVILLE SIGNAL SYSTEM.

SIGNAL HEAD HOOK-UP CHART																
PHASE	1	2	3	4	5	6	7	8	2 PED	4 PED	6 PED	8 PED	OLA	OLB	OLC	OLD
SIGNAL HEAD NO.	NU	NU	NU	41,42	NU	61,62	62	71	81,82	NU	NU	NU	NU	NU	NU	71*
RED				4R		6R		*	8R							
YELLOW				4Y		6Y			8Y							
GREEN				4G		6G			8G							
RED ARROW																
YELLOW ARROW							7Y									16R
FLASHING YELLOW ARROW																16Y
GREEN ARROW							7G	7G								16G

NU = Not Used
* Denotes install load resistor, see load resistor installation detail this sheet.
*See pictorial of head wiring detail this sheet.

DETECTOR RACK SET-UP DETAIL

INSERT DETECTOR CARDS IN RACK ACCORDING TO THE DETAIL SHOWN BELOW. PARTICULAR DETECTOR CHANNELS WILL CALL PHASES INDICATED.

DETECTOR RACK #1										
BIU	SLOT		SLOT		SLOT		CH1	CH1	SLOT	
	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	L9 ø4	L15 ø6	EMPTY	EMPTY
							CH2 L10 ø4	CH2 L16 ø6		

DETECTOR RACK #2				
BIU	CH1	CH1	SLOT	
	L19 ø8	L17 ø7	EMPTY	EMPTY
	CH2 L20 ø8	CH2 L18 ø4	EMPTY	EMPTY

WIRE LOOPS TO TERMINALS ON LOOP PANEL AS SHOWN IN THE CHART BELOW

LOOP NO.	LOOP PANEL TERMINALS
NU	L1A,L1B
NU	L2A,L2B
NU	L3A,L3B
NU	L4A,L4B
NU	L5A,L5B
NU	L6A,L6B
NU	L7A,L7B
NU	L8A,L8B
4A	L9A,L9B
4B	L10A,L10B
NU	L11A,L11B
NU	L12A,L12B
NU	L13A,L13B
NU	L14A,L14B
6A	L15A,L15B
6B	L16A,L16B
7A	L17A,L17B
	L18A,L18B
8A	L19A,L19B
8B	L20A,L20B
NU	L21A,L21B
NU	L22A,L22B
NU	L23A,L23B
NU	L24A,L24B

ADD JUMPERS FROM L17A TO L18A AND L17B TO L18B

NOTE
BE SURE TO PROGRAM DETECTOR TYPES AND TIMERS (EXTEND AND DELAY) AS SHOWN ON THE SIGNAL PLANS.

NU = NOT USED

PROGRAM CONTROLLER DETECTORS ACCORDING TO THE SCHEDULE SHOWN IN THE CHART BELOW

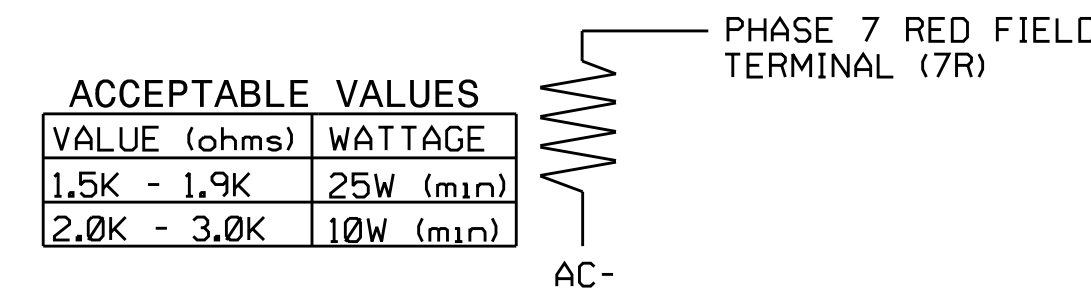
CONTROLLER DETECTOR NO.	FUNCTION	TIMING	
		FEATURE	TIME(SEC)
1	-	-	-
2	-	-	-
3	-	-	-
4	-	-	-
5	-	-	-
6	-	-	-
7	-	-	-
8	-	-	-
9	ø4	-	-
10	ø4	-	-
11	-	-	-
12	-	-	-
13	-	-	-
14	-	-	-
15	ø6	-	-
16	ø6	-	-
17	ø7	DELAY	15
18	ø4	-	-
19	ø8	-	-
20	ø8	DELAY	10
21	-	-	-
22	-	-	-
23	-	-	-
24	-	-	-

EQUIPMENT INFORMATION

CONTROLLER.....ASC/3
CABINETNC-8A [TS-2]
SOFTWAREECONOLITE ASC/ 2070
CABINET MOUNT.....BASE
LOADBAY POSITIONS.....16
LOAD SWITCHES USED.....4,6,7,8,16
PHASES USED.....4,6,7,8
OLD.....*

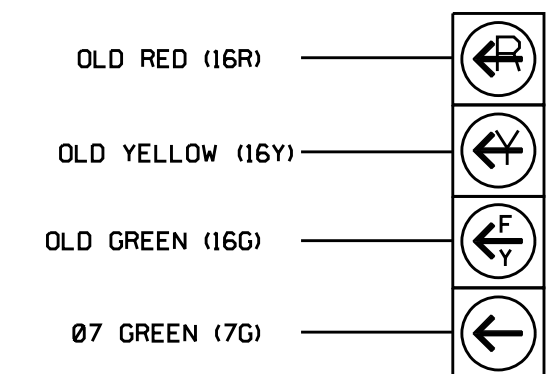
* See Sheet 2 of 2 Econolite ASC/2070 Overlap Programming Detail.

LOAD RESISTOR INSTALLATION DETAIL



4 SECTION FYA PPLT SIGNAL WIRING DETAIL

(wire signal heads as shown)



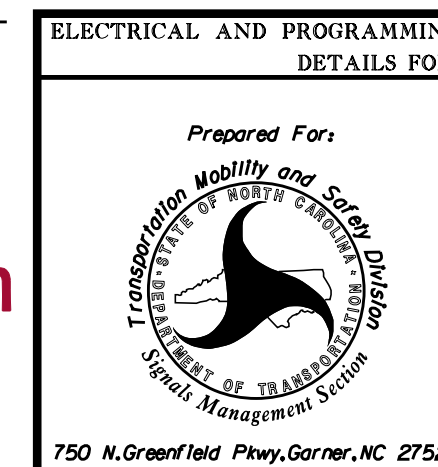
NOTE
1. SEE OVERLAP PROGRAMMING INSTRUCTIONS SHEET 2 OF 2.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 02-0016T2
DESIGNED: JUNE 2014
SEALED: 9/2/2014
REVISED: N/A

TEMPORARY DESIGN 2 - TMP PHASE 2

SHEET 1 OF 2

PLANS PREPARED IN THE OFFICE OF:
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SSR 1598 (10th STREET) AT SR 1702 (EVANS STREET)	
PLAN DATE: JUNE 2014	REVIEWED BY: SL PHILLIPS
PREPARED BY: SP PENNINGTON	REVIEWED BY:
REVISIONS	INIT. DATE

SEAL
NORTH CAROLINA PROFESSIONAL ENGINEER
SEAL 032607
STACIE L. PHILLIPS
DocuSigned by:
Stacie Phillips
9/2/2014
SIGNATURE DATE
SIG. INVENTORY NO. 02-0016T2