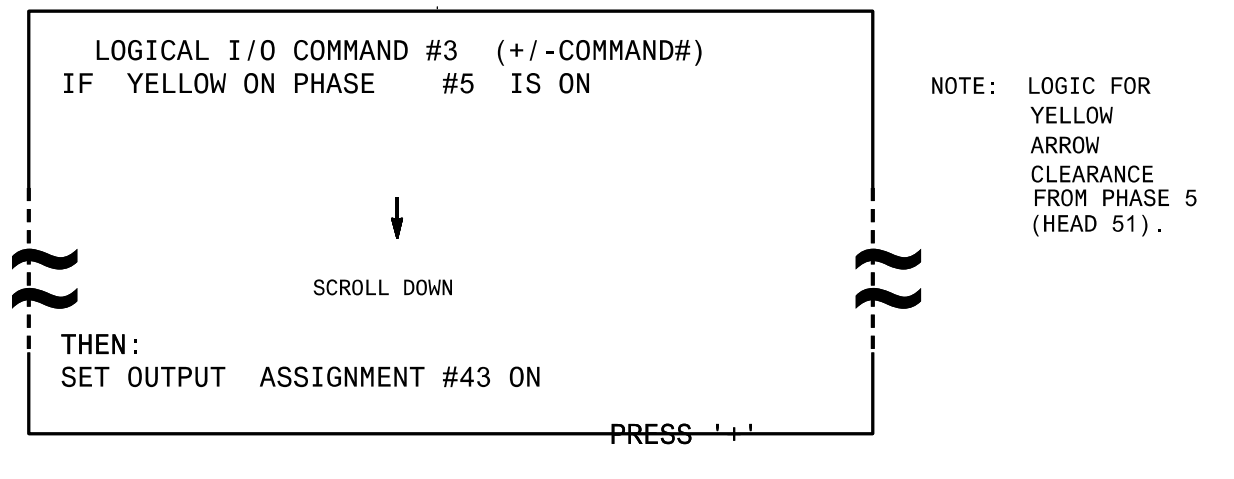
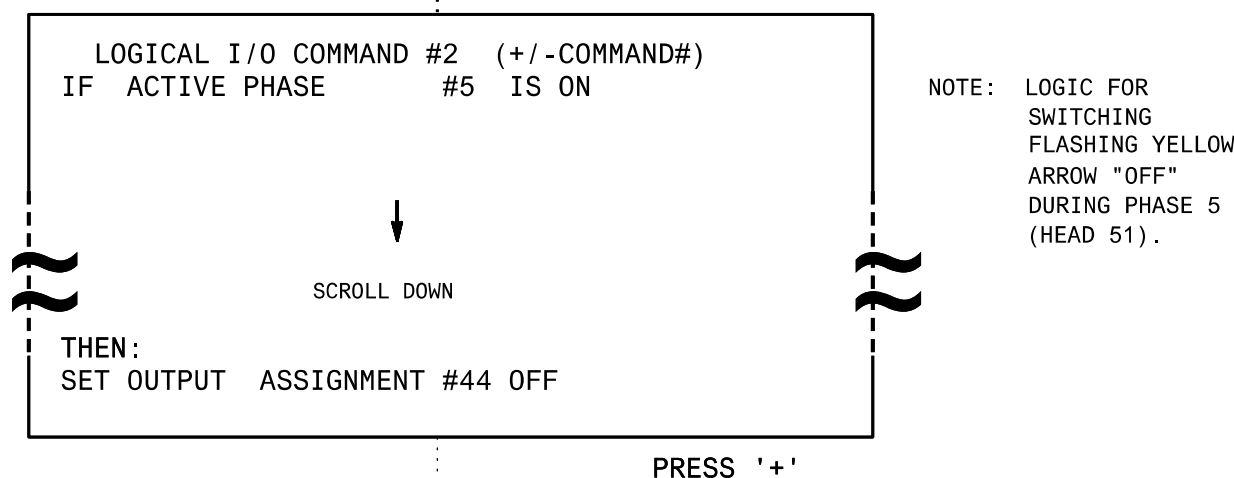
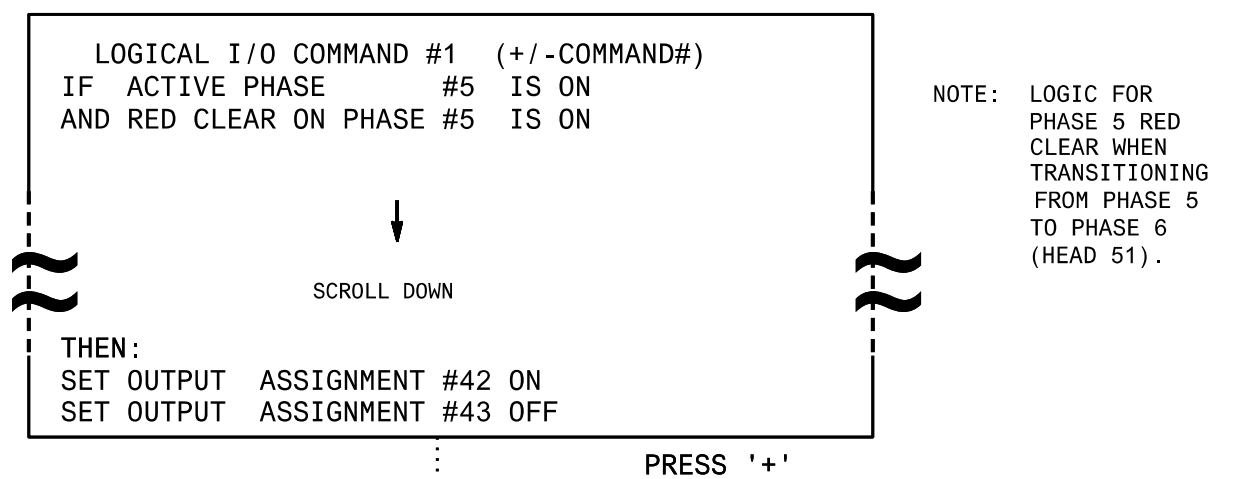


**LOGICAL I/O PROCESSOR PROGRAMMING DETAIL
TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE**

(program controller as shown below)

- FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2 AND 3.
- FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OUTPUT REFERENCE SCHEDULE

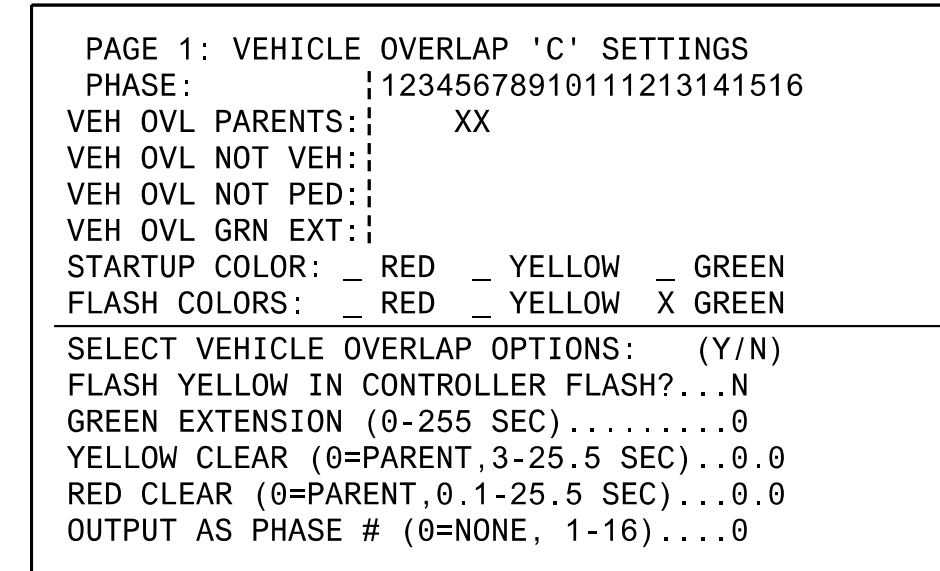
OUTPUT 42 = Overlap C Red
OUTPUT 43 = Overlap C Yellow
OUTPUT 44 = Overlap C Green

OVERLAP PROGRAMMING DETAIL

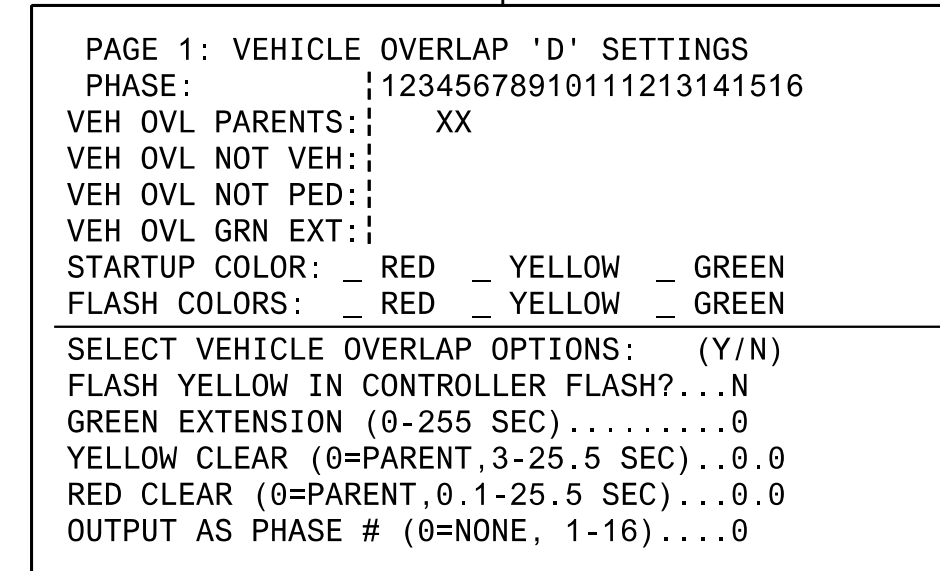
(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

PRESS '+' TWICE




PRESS '+'



OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 09-0651T1
DESIGNED: November 2025
SEALED: 02-12-26
REVISED: N/A

Electrical Detail - Sheet 2 of 2

<p>ELECTRICAL AND PROGRAMMING DETAILS FOR:</p> <p>Prepared in the Offices of:</p>  <p>750 N. Greenfield Pkwy, Garner, NC 27529</p>	<p>SR 4000 (University Parkway) at US 52 SB Ramps</p>		<p>SEAL 036880 ENGINEER KEITH M. MILES</p>
	<p>Division 9 Forsyth County Winston-Salem</p> <p>PLAN DATE: February 2026 REVIEWED BY:</p> <p>PREPARED BY: James Peterson REVIEWED BY:</p> <p>REVISIONS</p>	<p>INIT. DATE</p>	

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED