DocuSign Envelope ID: A5BCDB36-D4D6-48DB-920C-C1B77A8BD1EE

PROJECT REFERENCE NO.	SHEET NO.
C-5621	Sig. 3.2

ECONOLITE ASC/3-2070 OVERLAP PROGRAMMING DETAIL

(program controller as shown)

1. From Main Menu select [2. CONTROLLER]
2. From CONTROLLER Submenu select [2. VEHICLE OVERLAPS]
3. Press "Toggle" until positioned on Overlap G

OVERLAP G

Select TMG VEH OVLP [G] and 'NORMAL'

```
TMG VEH OVLP...[G] TYPE: .....NORMAL

PHASES 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
INCLUDED. . X . . . . . . . . . . . . .



LAG GRN 0.0  YEL 0.0  RED  0.0
```

Press Toggle until positioned over Overlap A

OVERLAP A

Select TMG VEH OVLP [A] and 'PPLT FYA'

```
TMG VEH OVLP...[A] TYPE: .....PPLT FYA

PROTECTED LEFT TURN....   PHASE    1
OPPOSING THROUGH.......   PHASE    2

FLASHING ARROW OUTPUT.....CH9  ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE........... 0
```

Toggle Once

OVERLAP B

Select TMG VEH OVLP [B] and 'PPLT FYA'

```
TMG VEH OVLP...[B] TYPE: .....PPLT FYA

PROTECTED LEFT TURN....   OVERLAP  G
OPPOSING THROUGH.......   PHASE    6

FLASHING ARROW OUTPUT.....CH10 ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE........... 0
```

Toggle Once

OVERLAP C

Select TMG VEH OVLP [C] and 'PPLT FYA'

```
TMG VEH OVLP...[C] TYPE: .....PPLT FYA

PROTECTED LEFT TURN....   PHASE    5
OPPOSING THROUGH.......   PHASE    6

FLASHING ARROW OUTPUT.....CH11 ISOLATE

DELAY START OF: FYA..0.0 CLEARANCE..0.0
ACTION PLAN SF BIT DISABLE........... 0
```

Toggle Once

ECONOLITE ASC/3-2070 LOGIC PROCESSOR PROGRAMMING FOR FYA SUPPRESSION DURING THE DELAYED GREEN PERIOD

(program controller as shown)

1. From Main Menu select [1. CONFIGURATION]
2. From CONFIGURATION Submenu select [8. LOGIC PROCESSOR]
3. From LOGIC PROCESSOR Submenu select [2. LOGIC STATEMENTS]

ENTER A "1" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:   1  COPY FROM:   1  ACTIVE:  M   (T/F)
IF     PED ON PH WALK        6     IS   ON
AND    VEH GREEN ON PH       6     IS   OFF

THEN   SIG SET OLP RED       2          ON
       SIG SET OLP YELLOW    2          OFF
       SIG SET OVLP GREEN    2          OFF

ELSE
```

LOGIC STATEMENT FOR ADVANCE WALK WITH FYA'S. TURN FYA HEAD 63 OFF DURING PED 6 ADVANCE WALK.

END PROGRAMMING

1. From Main Menu select [1. CONFIGURATION]
2. From CONFIGURATION Submenu select [8. LOGIC PROCESSOR]
3. From LOGIC PROCESSOR Submenu select [1. LOGIC STATEMENT CONTROL]

ENABLE LOGIC PROCESSOR STATEMENT 1 BY POSITIONING THE CURSOR OVER THE FIELDS SHOWN BELOW AND USING THE TOGGLE KEY TO ENABLE IT.

```
LOGIC STATEMENT CONTROL
          1 2 3 4 5 6 7 8 9 0 1 2 3 4 5
LP 1-15   E . . . . . . . . . . . . . .
LP 16-30  . . . . . . . . . . . . . . .
LP 31-45  . . . . . . . . . . . . . . .
LP 46-60  . . . . . . . . . . . . . . .
LP 61-75  . . . . . . . . . . . . . . .
LP 76-90  . . . . . . . . . . . . . . .
```

END PROGRAMMING

OVERLAP D

Select TMG VEH OVLP [D] and 'NORMAL'

```
TMG VEH OVLP...[D] TYPE: .....NORMAL

PHASES 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
INCLUDED. X . X . . . . . . . . . . . .



LAG GRN 0.0  YEL 0.0  RED  0.0
```

Toggle Once

OVERLAP E

Select TMG VEH OVLP [E] and 'NORMAL'

```
TMG VEH OVLP...[E] TYPE: .....NORMAL

PHASES 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
INCLUDED. . X . . . . . . . . . . . . .



LAG GRN 0.0  YEL 0.0  RED  0.0
```

END PROGRAMMING

ECONOLITE ASC/3-2070 LOAD SWITCH ASSIGNMENT DETAIL

(program controller as shown)

To assign load switch S4 as OLG, program LD SWITCH 3 as OVLP '7' TYPE 'O' as shown below.

1. From Main Menu select [1. CONFIGURATION]
2. From CONFIGURATION Submenu select [3. LOAD SW ASSIGN]

NOTICE OVLP 7 ASSIGNED TO LD SWITCH 3

LD SWITCH ASSIGN

	PHASE /OVLP	TYPE	DIMMING R	Y	G	D	---FLASH--- PWR	AUT	TGR
1	1	V	.	.	.	+	A	R	X
2	2	V	.	.	.	+	A	Y	.
3	7	O	.	.	.	+	A	R	X
4	4	V	.	.	.	+	A	R	.
5	5	V	.	.	.	−	A	R	.
6	6	V	.	.	.	−	A	Y	X
7	7	V	.	.	.	−	A	R	.
8	8	V	.	.	.	−	A	R	X
9	1	O	.	.	.	+	A	Y	X
10	2	O	.	.	.	+	A	R	X
11	3	O	.	.	.	−	A	Y	.
12	4	O	.	.	.	−	A	Y	.
13	2	P	.	.	.	+	A	.	.
14	4	P	.	.	.	−	A	.	.
15	6	P	.	.	.	+	A	.	.
16	8	P	.	.	.	−	A	.	.

FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO ENSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

1. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
2. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

This plan supersedes the electrical plan signed and sealed by Steven G. Haynie, PE on 05/31/2022.

Temporary Signal 2 - TCP Phase 2
Electrical Detail Sheet - 2 of 2

THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 10-0885T2
DESIGNED: February 2023
SEALED: February 21, 2023
REVISED: N/A

RS&H
NC FIRM LICENSE No: F-0493
8521 SIX FORKS ROAD, SUITE 400
RALEIGH, NC 27615
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DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED

Prepared for the Offices of:
Traffic Engineering, Mobility and Safety Division
Department of Transportation
Signals Management Section
750 N.Greenfield Pkwy,Garner,NC 27529

US 21 (Catawba Avenue)/ Catawba Avenue at US 21 (Statesville Road)/ Holiday Lane

Division 10 Mecklenburg County Cornelius

PLAN DATE:	March 2023	REVIEWED BY:	V. Kaiser
PREPARED BY:	S.G. Haynie	REVIEWED BY:	

REVISIONS	INIT.	DATE

SEAL
NORTH CAROLINA PROFESSIONAL SEAL 029531 ENGINEER STEVEN G. HAYNIE

DocuSigned by: Steven G. Haynie 3/8/2023
DESIGN ENGINEER SIGNATURE DATE

Sig. Inventory No. 10-0885T2

3/8/2023
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