LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, AND 12.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).

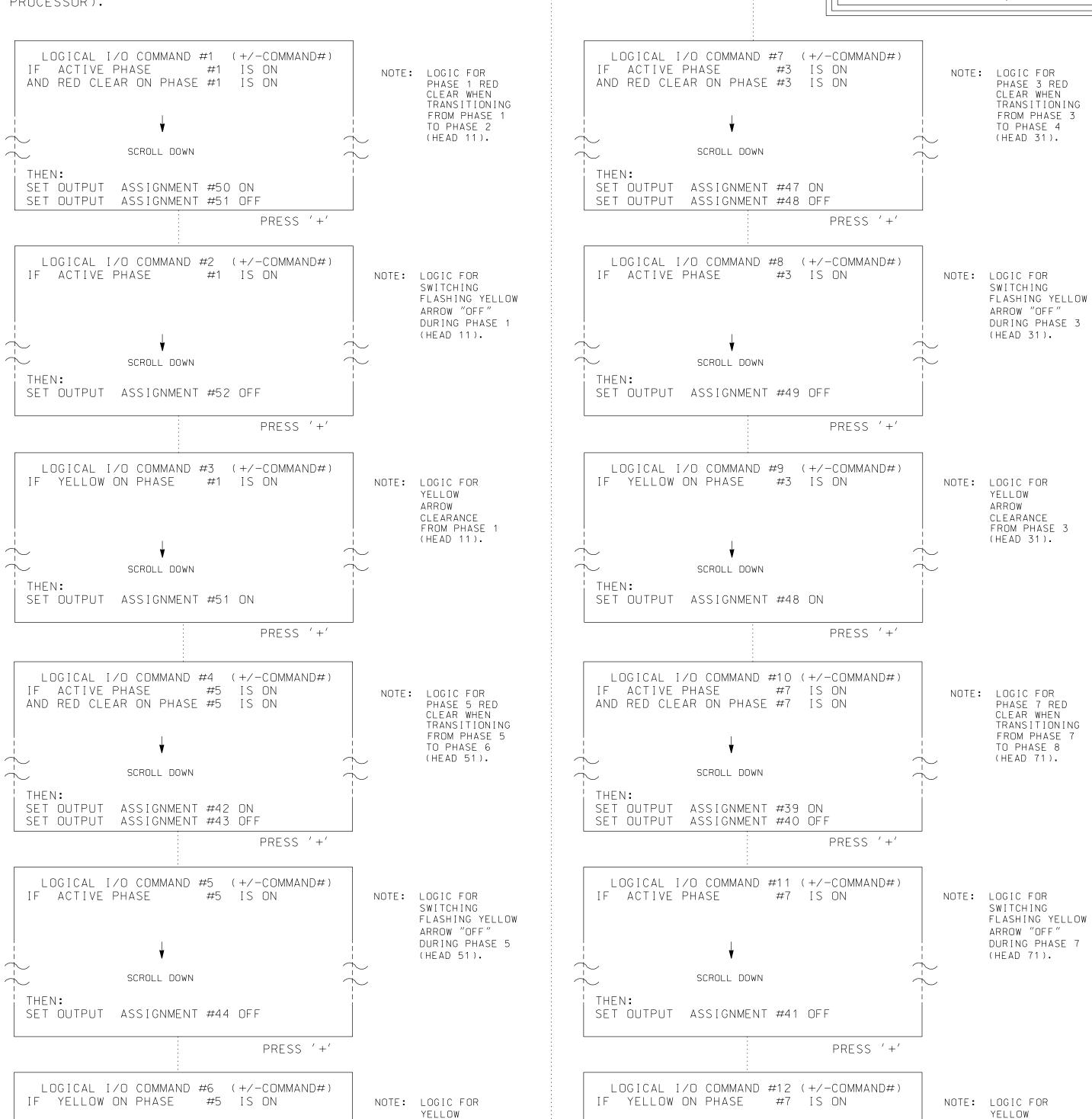
OUTPUT REFERENCE SCHEDULE USE TO INTERPRET LOGIC PROCESSOR OUTPUT 39 = Overlap D Red OUTPUT 40 = Overlap D Yellow OUTPUT 41 = Overlap D Green OUTPUT 42 = Overlap C Red OUTPUT 43 = Overlap C Yellow OUTPUT 44 = Overlap C Green OUTPUT 47 = Overlap B Red OUTPUT 48 = Overlap B Yellow OUTPUT 49 = Overlap B Green OUTPUT 50 = Overlap A Red OUTPUT 51 = Overlap A Yellow OUTPUT 52 = Overlap A Green

ARROW

CLEARANCE

(HEAD 71).

FROM PHASE



ARROW

CLEARANCE

(HEAD 51).

FROM PHASE 5

SCROLL DOWN

LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

SET OUTPUT ASSIGNMENT #40 ON

OVERLAP PROGRAMMING DETAIL FOR DEFAULT PHASING

GREEN

FLASH

← NOTICE

GREEN

FLASH

FROM MAIN MENU PRESS '8' (OVERLAPS),

THEN '1' (VEHICLE OVERLAP SETTINGS).

¦12345678910111213141516

PRESS '+'

PRESS '+'

12345678910111213141516

PAGE 1: VEHICLE OVERLAP 'A' SETTINGS

STARTUP COLOR: _ RED _ YELLOW _ GREEN

SELECT VEHICLE OVERLAP OPTIONS: (Y/N)

FLASH YELLOW IN CONTROLLER FLASH?...Y

OUTPUT AS PHASE # (0=NONE, 1-16)....0

PAGE 1: VEHICLE OVERLAP 'B' SETTINGS

STARTUP COLOR: _ RED _ YELLOW _ GREEN

SELECT VEHICLE OVERLAP OPTIONS: (Y/N)

YELLOW CLEAR (O=PARENT,3-25.5 SEC)..0.0

RED CLEAR (0=PARENT,0.1-25.5 SEC)...0.0

FLASH YELLOW IN CONTROLLER FLASH?...N

GREEN EXTENSION (0-255 SEC).....

OUTPUT AS PHASE # (0=NONE, 1-16)....0

FLASH COLORS: _ RED _ YELLOW X GREEN

GREEN EXTENSION (0-255 SEC).....0

YELLOW CLEAR (O=PARENT,3-25.5 SEC)..O.O

RED CLEAR (0=PARENT, 0.1-25.5 SEC)...0.0

PHASE:

VEH OVL PARENTS: XX

VEH OVL PARENTS: XX

VEH OVL NOT VEH:

VEH OVL NOT PED:

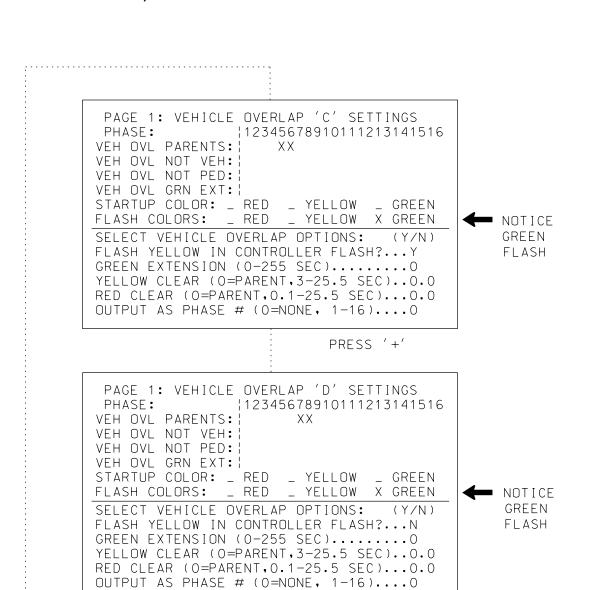
VEH OVL GRN EXT: |

VEH OVL NOT VEH: |

VEH OVL GRN EXT: |

VEH OVL NOT PED:

(program controller as shown below)



OVERLAP PROGRAMMING COMPLETE

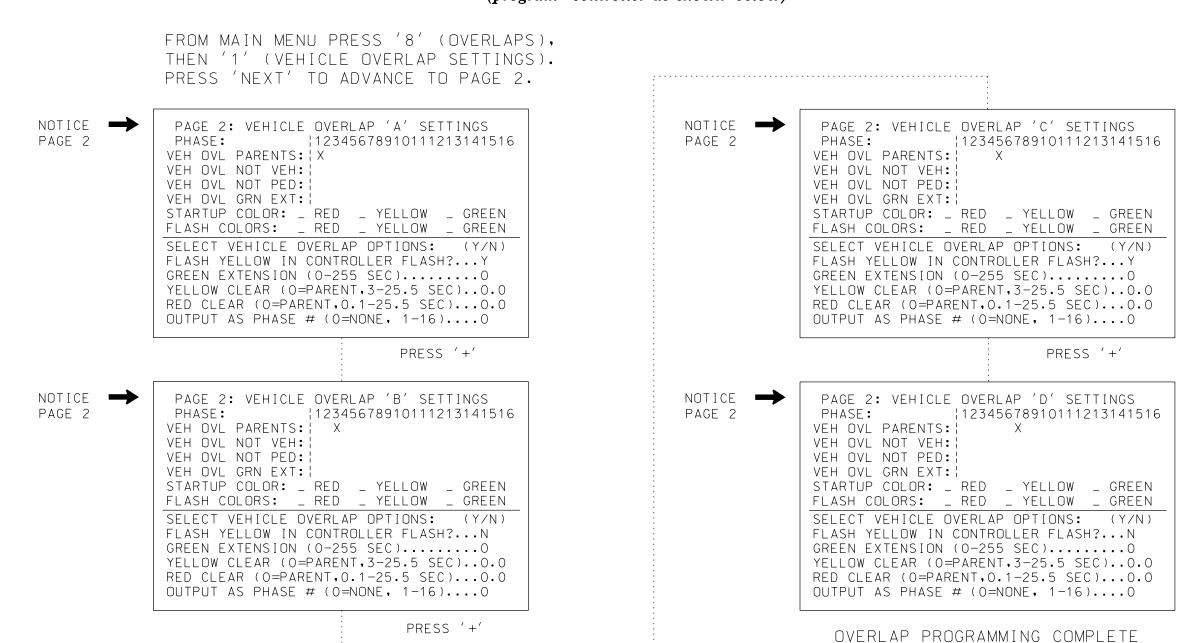
PROJECT REFERENCE NO.

U-5775

Sig.3.2

OVERLAP PROGRAMMING DETAIL FOR ALTERNATE PHASING

(program controller as shown below)





Electrical Detail-Final Design-Sheet 2 of 9

ELECTRICAL AND PROGRAMMING DETAILS FOR

750 N.Greenfield Pkwy, Garner, NC 27529

US 74 Bus. (Marion Street) Prepared for the Offices of:

NC 150 (Cherryville Road) SR 2053 (Peach Street)

Division 12 Cleveland County Shelby PLAN DATE: March 2022 REVIEWED BY: J.L. Lewis PREPARED BY: J. Ma REVIEWED BY: M.L. Stygles REVISIONS INIT. DATE

VHB Engineering NC, P.C. (C-3705) 940 Main Campus Drive, Suite 500 Raleigh, NC 27607 P: 919-829-0328 **DOCUMENT NOT CONSIDERED** FINAL UNLESS ALL SIGNATURES COMPLETED SEAL 033108 MIXN Jianzin Ma

\$75F185308A44F...

SIG. INVENTORY NO.

DATE 12-0600

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 12-0600 DESIGNED: March 2022 SEALED: 03/01/2022 REVISED: N/A

SCROLL DOWN

PRESS '+'

SET OUTPUT ASSIGNMENT #43 ON