## ECONOLITE ASC/3-2070 OVERLAP PROGRAMMING DETAIL

(program controller as shown)

- 1. From Main Menu select | 2. CONTROLLER
- 2. From CONTROLLER Submenu select | 2. VEHICLE OVERLAPS

Toggle Once

OVERLAP B

Select TMG VEH OVLP [B] and 'PPLT FYA'

TMG VEH OVLP...[B] TYPE: .... PPLT FYA PROTECTED LEFT TURN.... PHASE 3 OPPOSING THROUGH..... PHASE 4 FLASHING ARROW OUTPUT....CH10 ISOLATE DELAY START OF: FYA..O.O CLEARANCE..O.O ACTION PLAN SF BIT DISABLE..... 0 Toggle Twice

OVERLAP D

Select TMG VEH OVLP [D] and 'PPLT FYA'

TMG VEH OVLP...[D] TYPE: .... PPLT FYA PROTECTED LEFT TURN.... PHASE 7 OPPOSING THROUGH..... PHASE 8 FLASHING ARROW OUTPUT....CH12 ISOLATE DELAY START OF: FYA..O.O CLEARANCE..O.O ACTION PLAN SF BIT DISABLE..... 0

END PROGRAMMING

## ECONOLITE ASC/3-2070 PREEMPT FILTERING PROGRAMMING DETAIL

(program controller as shown)

- 1. From Main Menu select 4. PREEMPTOR/TSP
- 2. From PREEMPT/TSP/SCP Submenu select | 2. ENABLE PREEMPT FILTERING & TSP/SCP

ENABLE PREEMPT FILTERING & TSP/SCP FILTERED SOLID PULSING INPUT 1 ...BYPASSED.. ...BYPASSED.. 2 ...BYPASSED.. ...BYPASSED.. 3 .. PREEMPT 3. ... BYPASSED.. 4 ..PREEMPT 4. ...BYPASSED.. 5 .. PREEMPT 5. ... BYPASSED.. 6 .. PREEMPT 6. ... BYPASSED.. 7 ...BYPASSED.. ...BYPASSED.. 8 ...BYPASSED.. ...BYPASSED.. 9 ...BYPASSED.. ...BYPASSED.. 10 ...BYPASSED.. ...BYPASSED..

## ECONOLITE ASC/3-2070 LOGIC PROCESSOR PROGRAMMING DETAIL FOR PREEMPT ONLY PHASE OMIT

(program controller as shown)

The following logic processor configuration holds the FYA's on signal heads 11, 31, 51, and 71 red for the duration of the delayed green time (leading ped interval) when serving a ped call on the opposing through phase.

- 1. From Main Menu select | 1. CONFIGURATION
- 2. From CONFIGURATION Submenu select 8. LOGIC PROCESSOR
- 3. From the LOGIC PROCESSOR Submenu select 2. LOGIC STATEMENTS

ENTER A "1" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#: 1 COPY FROM: 1 ACTIVE: M (T/F) IF PMT PREEMPT ACTIVE 5 IS OFF THEN CTR OMIT PHASE ELSE

LOGIC FOR OMMITTING PHASE 3 AT STARTUP AND/OR WHEN NOT IN PREEMPT

4. From the LOGIC PROCESSOR Submenu select 1. LOGIC STATEMENT CONTROL

ENABLE LOGIC PROCESSOR STATEMENTS 1-4 BY POSITIONING THE CURSOR OVER THE FIELDS SHOWN BELOW AND USING THE TOGGLE KEY TO ENABLE THEM .

LOGIC STATEMENT CONTROL 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 

END PROGRAMMING

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: Ø1-ØØ13 DESIGNED: MARCH 2018 SEALED: 08/21/2018 REVISED: N/A

Electrical Detail - Sheet 2 of 4

ELECTRICAL AND PROGRAMMING

US 17 (Hughes Blvd.) SR 1309 (W. Main St.)/ W. Main St.

Division 1 Pasquotank County Elizabeth City PLAN DATE: March 2018 REVIEWED BY: AJ Davis

DJ White REVIEWED BY: PREPARED BY: LM Moon REVISIONS INIT. DATE Lisa M. Moon 9/20/2018

SIG. INVENTORY NO. 01-0013

**DOCUMENT NOT CONSIDERED** 

FINAL UNLESS ALL SIGNATURES COMPLETED



