R-4707 Sig. 13.

ECONOLITE ASC/3-2070 LOGIC PROCESSOR PROGRAMMING DETAIL

(program controller as shown)

THIS LOGIC PROCESSOR PROGRAMMING PROVIDES ADDITIONAL RED CLEARANCE FOR THE TRANSISTION TO PHASE 8 FROM PHASE 6 BY FORCING THE CONTROLLER TO SERVE PHASE 7 FIRST. THIS IS NECESSARY DUE TO THE LONG THROAT DISTANCE BETWEEN THE TWO MOVEMENTS.

- 1. From Main Menu select 1. CONFIGURATION
- 2. From CONFIGURATION Submenu select 8. LOGIC PROCESSOR
- 3. From LOGIC PROCESSOR Submenu select 1. LOGIC STATEMENT CONTROL

ENABLE LOGIC PROCESSOR STATEMENTS 1 & 2 BY POSITIONING THE CURSOR OVER THE FIELDS SHOWN BELOW AND USING THE TOGGLE KEY TO ENABLE THEM.

LOGIC STATEMENT			CONTROL												
	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5
LP 1-15	Ε	Ε	•	•	•	•	•	•	•	•	•	•	•	•	•
LP 16-30	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
LP 31-45	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
LP 46-60	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
LP 61-75	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
LP 76-90	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

END PROGRAMMING

- 1. From Main Menu select 1. CONFIGURATION
- 2. From CONFIGURATION Submenu select 8. LOGIC PROCESSOR
- 3. From LOGIC PROCESSOR Submenu select | 2. LOGIC STATEMENTS

ENTER A "1" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#: 1 COPY FROM: 1 ACTIVE:M (T/F)

IF CTR PHASE TIMING 6 IS ON

THEN CTR OMIT PHASE 8 ON

ELSE

ENTER A "2" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

LP#: 2 COPY FROM: 2 ACTIVE:M (T/F)

IF CTR ON PHASE CHECK 8 IS ON

OR CTR ON PH PED CHK 8 IS ON

THEN CTR CALL PHASE 7 ON

ELSE

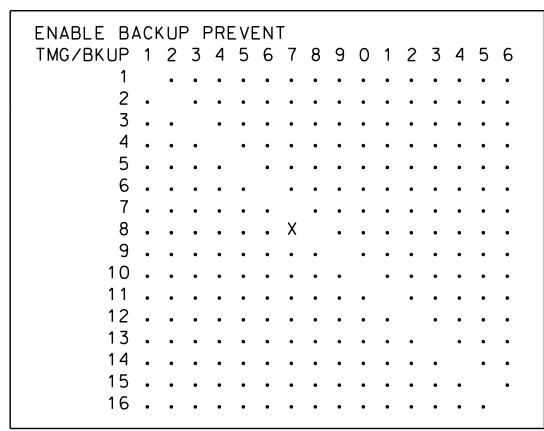
END PROGRAMMING

ECONOLITE ASC/3-2070 BACKUP PROTECTION ENABLE PROGRAMMING

(program controller as shown)

- 1. From Main Menu select 1. CONFIGURATION
- 2. From CONFIGURATION Submenu select 1. CONTROLLER SEQ
- 3. From CONTROLLER SEQUENCE Submenu select 3. BACKUP PREVENT PHASES

Follow programming as shown below. On the 'ENABLE BACKUP PREVENT' screen move cursor to the appropriate field and press 'YES/NO' on the controller keypad to toggle field value between 'X' .'B'. 'C' and 'OFF'.



END PROGRAMMING

NOTE

'X' inhibits the controller from servicing the 'BACKUP' (column) phase when the 'TIMING' (row) phase is active or next.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 07-0905T1 DESIGNED: April 2020 SEALED: April 20,2020 REVISED: N/A

Project #: 180914



Electrical Detail - Sheet 2 of 2
Tempory Design 1 (TMP Phase III, Step 1)

ELECTRICAL AND PROGRAMMING
DETAILS FOR:



SR 4771 (Reedy Fork Parkway)
at

US 29 Northbound Ramp

Division 7 Guilford County Gre

PLAN DATE: April 2020 REVIEWED BY: R. Hinsh

PLAN DATE: April 2020 REVIEWED BY: R. Hinshaw
PREPARED BY: T.S. Warren REVIEWED BY:
REVISIONS INIT. DATE

SEAL
032117

Docusigned by:

Royal Hinsham

SIGNATURE

DATE

3EU34197604F492...

DATE

DOCUMENT NOT CONSIDERED

FINAL UNLESS ALL

SIGNATURES COMPLETED

INIT. DATE

DocuSigned by:

Signature

Date

SIGNATURE

DATE

SIGNATURE

SIGN