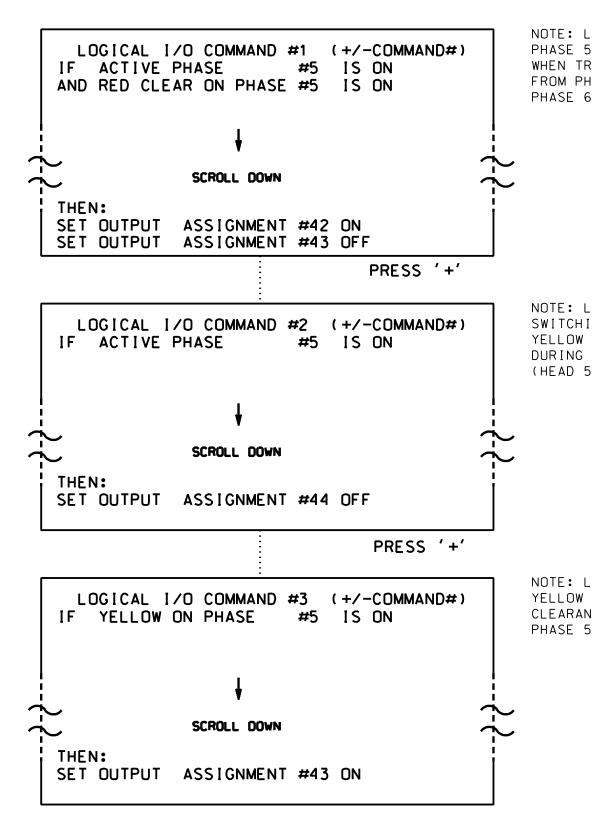
LOGICAL I/O PROCESSOR PROGRAMMING

TO PRODUCE SPECIAL FYA-PPLT SIGNAL

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE ENABLE ACT LOGIC COMMANDS 1, 2, and 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LC PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OUTPUT REFERENCE SCHEDULE
USE TO INTERPRET LOGIC PROCESSOR
OUTPUT 42 = Overlap C Red OUTPUT 43 = Overlap C Yellow OUTPUT 44 = Overlap C Green

	PROJECT REFERENCE NO.SHEET NO.R-1015Sig. 18.2
DETAIL	
SEQUENCE	
N '1' (PHASE	
HE MENU AND	
(LOGICAL I/O	
E: LOGIC FOR	
SE 5 RED CLEAR N TRANSITIONING M PHASE 5 TO	OVERLAP PROGRAMMING DETAIL
SE 6 (HEAD 51).	
	(program controller as shown below)
	FROM MAIN MENU PRESS '8' (OVERLAPS), THEN
	'1' (VEHICLE OVERLAP SETTINGS).
E: LOGIC FOR	PRESS '+' TWICE
TCHING FLASHING LOW ARROW OFF ING PHASE 5	PAGE 1: VEHICLE OVERLAP 'C' SETTINGS PHASE: \12345678910111213141516 VEH OVL PARENTS:\XX
AD 51).	VEH OVL NOT VEH: VEH OVL NOT PED:
	VEH OVL GRN EXT:¦ STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW X GREENNOTICE
	SELECT VEHICLE OVERLAP OPTIONS:(Y/N)GREENFLASH YELLOW IN CONTROLLER FLASH?YFLASHGREEN EXTENSION (0-255 SEC)0
	YELLOW CLEAR (0=PARENT,3-25.5 SEC)0.0 RED CLEAR (0=PARENT,0.1-25.5 SEC)0.0
E: LOGIC FOR	OUTPUT AS PHASE # $(0=NONE + 1-16) \dots 0$
LOW ARROW ARANCE FROM SE 5 (HEAD 51).	OVERLAP PROGRAMMING COMPLETE
	THIS ELECTRICAL DETAIL IS FOR
	THE SIGNAL DESIGN: 02-0904 DESIGNED: March 2018
	SEALED: 12-7-18 REVISED: N/A
	Electrical Detail - Sheet 2 of 2
	Signal Upgrade Unless all signatures completed Electrical and programming Details for: SR 1756 (Lake Road)
	Prepared for: at
	US 70 WB Ramp Division 02 Craven Co. Havelock
	PLAN DATE: March 2018 REVIEWED BY: A.D. Klinksiek
	REVISIONS INIT. DATE DocuSigned by: Raleigh, North Carolina 27609 Revisions
	NC License No: C-1554 750 N.Greenfield Pkwy.Garner.NC 27529 (919) 546-8997 DATE SIG. INVENTORY NO. 02-0904

