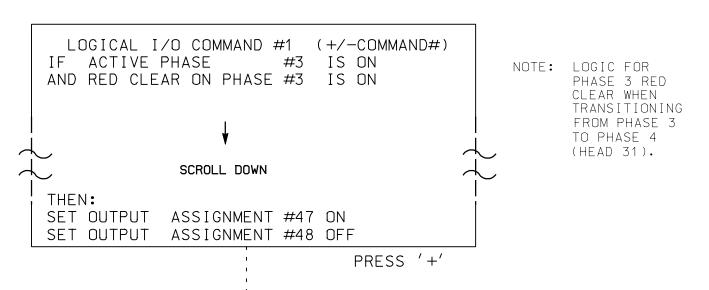
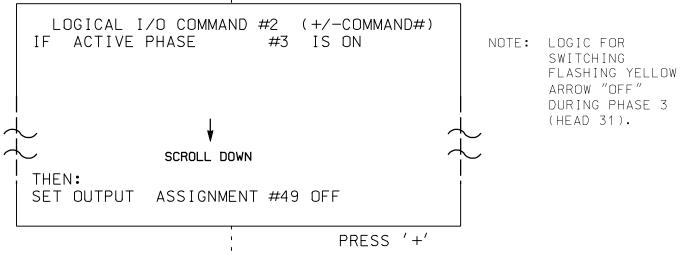
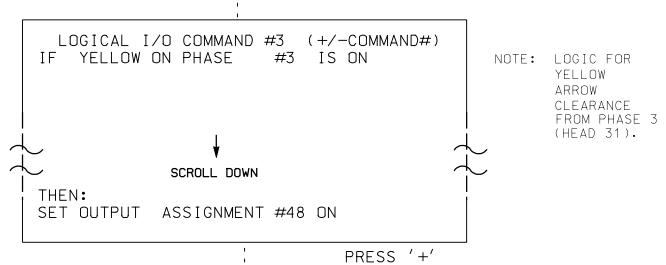
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

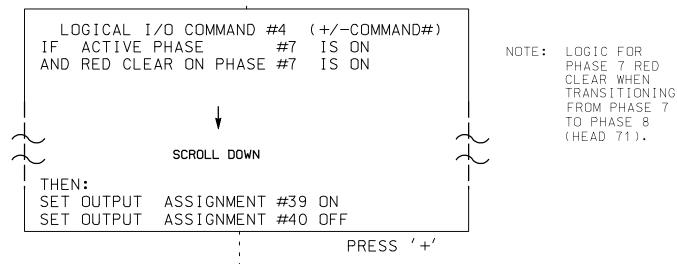
(program controller as shown below)

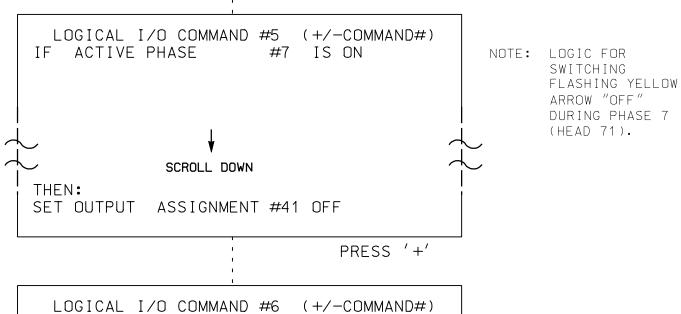
- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, AND 6.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).

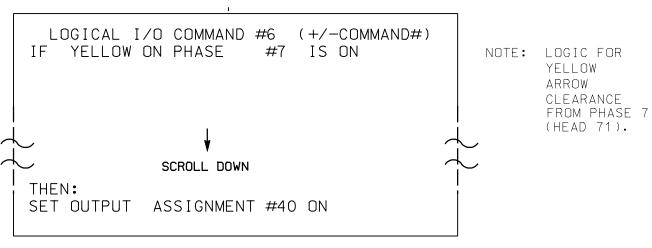












LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 14-0021 DESIGNED: December 2018 SEALED: Ø2/28/2019 REVISED: N/A

OUTPUT REFERENCE SCHEDULE

USE TO INTERPRET LOGIC PROCESSOR

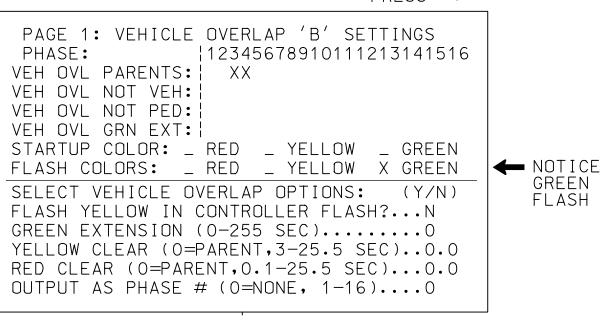
OUTPUT 39 = Overlap D Red OUTPUT 40 = Overlap D Yellow OUTPUT 41 = Overlap D Green OUTPUT 47 = Overlap B Red OUTPUT 48 = Overlap B Yellow OUTPUT 49 = Overlap B Green

OVERLAP PROGRAMMING DETAIL

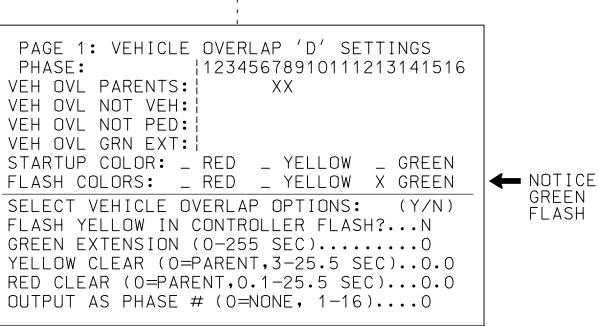
(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

PRESS '+'



PRESS '+' TWICE



OVERLAP PROGRAMMING COMPLETE

FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

- 1. ON REAR OF PDA REMOVE WIRE FROM TERM, T2-4 AND TERMINATE ON T2-2.
- 2. ON REAR OF PDA REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
- 3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

Electrical Details - Sheet 2 of 2 - Signal Modification

ELECTRICAL AND PROGRAMMING DETAILS FOR: Prepared in the Offices of:

750 N.Greenfield Pkwy, Garner, NC 27529

US 19/64/74/129 US 19 Bus/SR 1556 (Hiwassee St)

Division 14 Cherokee County Near Murphy PLAN DATE: December 2018 REVIEWED BY: Z Harris PREPARED BY: K M Cory REVIEWED BY: REVISIONS INIT. DATE

SEAL SEAL 038970

DOCUMENT NOT CONSIDERED

FINAL UNLESS ALL

SIGNATURES COMPLETED

Kelly M Cory 2/28/2019

SIGNATURE DATE SIG. INVENTORY NO. 14-0021

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