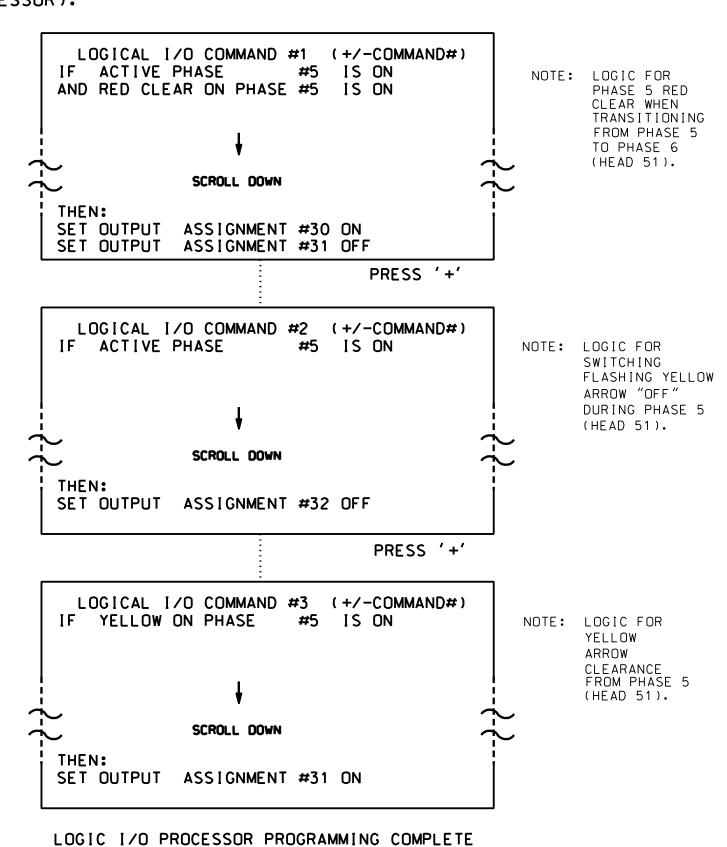
PROJECT REFERENCE NO. I-5714 / U-5114 | Sig. 16.

## LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, and 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



OUTPUT REFERENCE SCHEDULE

OUTPUT 30 = Overlap C Red OUTPUT 31 = Overlap C Yellow OUTPUT 32 = Overlap C Green

Note: All outputs shown above have been remapped. See sheet 3 of this electrical detail.

## OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS). THEN '1' (VEHICLE OVERLAP SETTINGS).

PRESS '+' TWICE

PAGE 1: VEHICLE OVERLAP 'C' SETTINGS 12345678910111213141516 PHASE: VEH OVL PARENTS: | XX VEH OVL NOT VEH: | VEH OVL NOT PED: : VEH OVL GRN EXT: : STARTUP COLOR: \_ RED \_ YELLOW \_ GREEN NOTICE GREEN FLASH FLASH COLORS: \_ RED \_ YELLOW X GREEN SELECT VEHICLE OVERLAP OPTIONS: (Y/N) FLASH YELLOW IN CONTROLLER FLASH?...Y GREEN EXTENSION (0-255 SEC).....0 YELLOW CLEAR (O=PARENT.3-25.5 SEC)..O.O RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)....0

OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 10-1619T2 DESIGNED: December 2017 SEALED: 04-23-2018 REVISED: N/A

Electrical Detail - Sheet 2 of 3

Signal Upgrade Temporary Design 2

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



SR 2136 (Gilead Road) I-77 NB Ramps

Division 10 Mecklenburg Co. Huntersville December 2017 REVIEWED BY: A.D. Klinksiek PLAN DATE: PREPARED BY: A.H. Thornburg REVIEWED BY: N.R. Simmons REVISIONS INIT. DATE

SIG. INVENTORY NO. 10-1619

SEAL 031464

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